

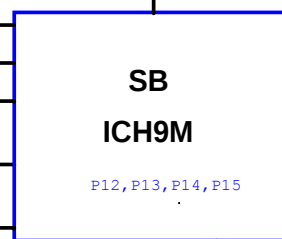
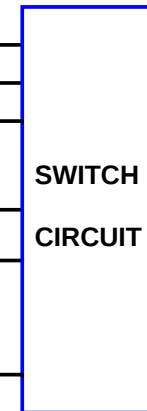
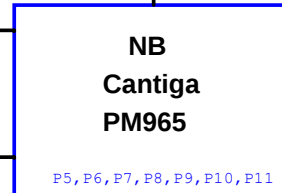
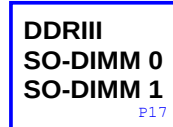
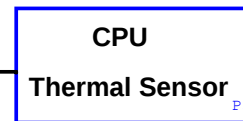
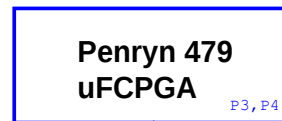
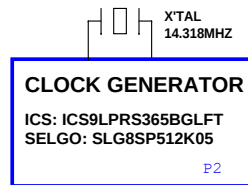
ZY2 SYSTEM BLOCK DIAGRAM

BOM MARK

E@ EXT VGA 要打
268@ AUDIO 268 要打
D@ DOCK
D2@ DDR2 要打
SP@ 特殊(EXT VGA OR DDR2)
LC@ LOW COST 要打
ED2@ EXT VGA & DDR2 要打
CB@ CARDBUS 要打
NSF@ Non ASF 要打

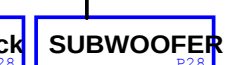
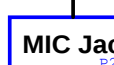
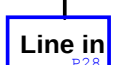
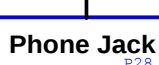
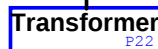
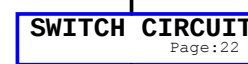
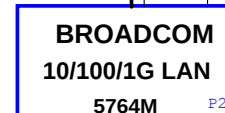
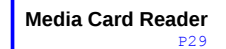
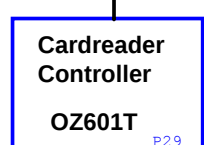
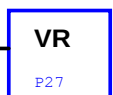
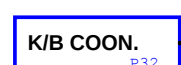
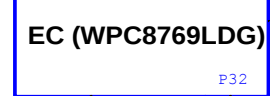
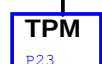
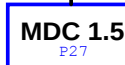
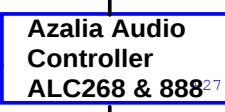
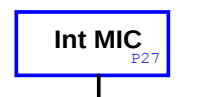
I@ INT VGA 要打
888@ AUDIO 888 要打
D3@ DDR3 要打
ND@ NON DOCK 要打
NLC@ NON LOW COST 要打
TPM@ INT TPM
ID2@ INT VGA & DDR2 要打
ED3@ EXT VGA & DDR3 要打
ID3@ INT VGA & DDR3 要打
ASF@ ASF 要打
NCB@ NON CARDBUS 要打

LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI

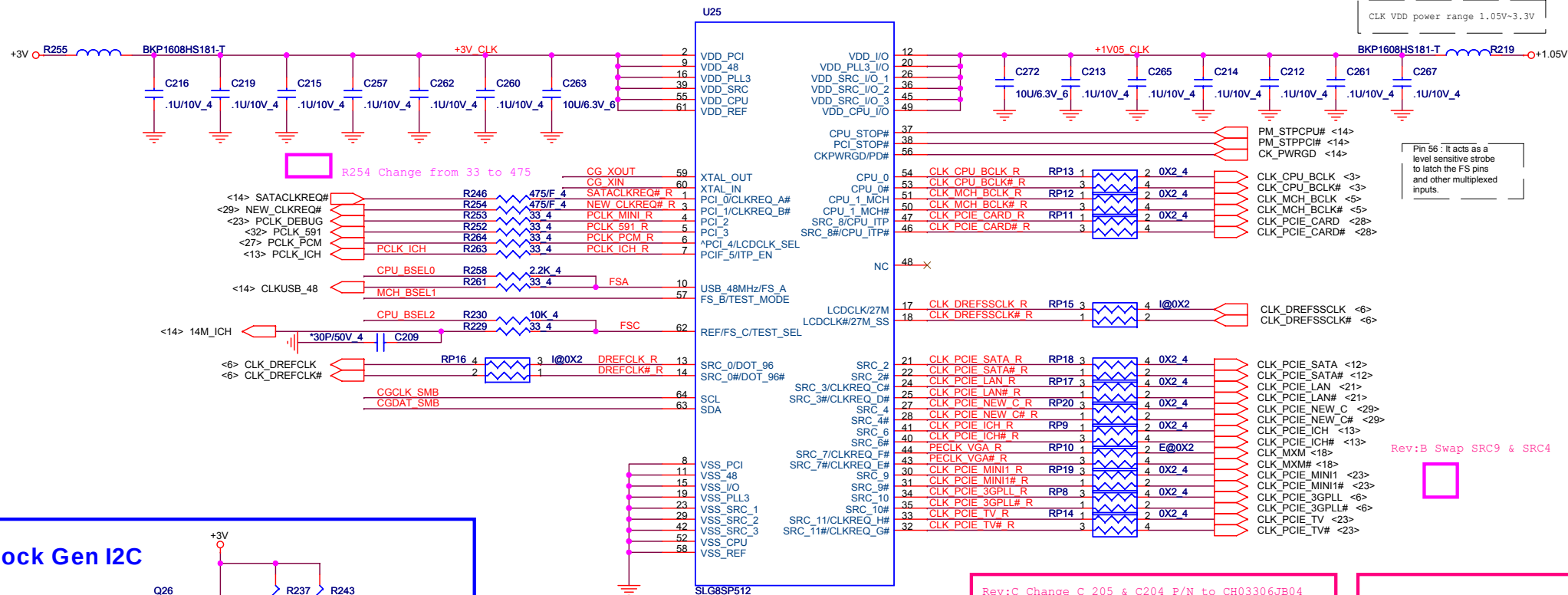


PCI-Express

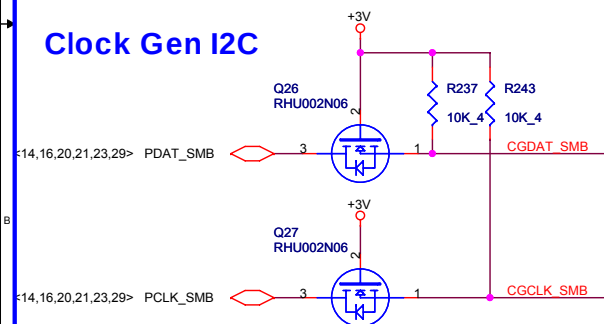
PCI-E-1



Clock Generator

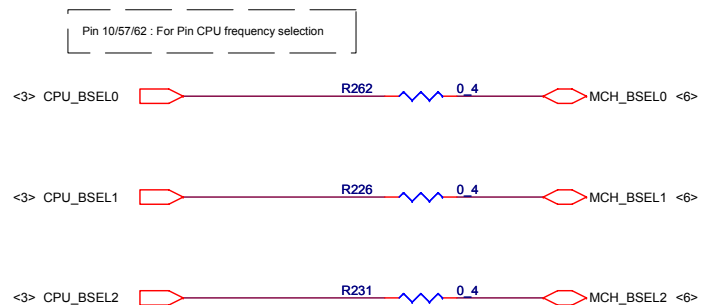


Clock Gen I2C



	QCI P/N
SLG8SP512	AL8SP512K05
ICS9LPRS365BGLFT	ALPRS365K13

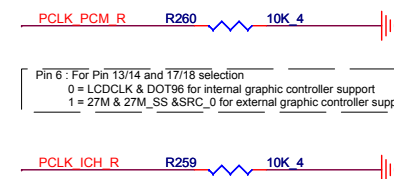
CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



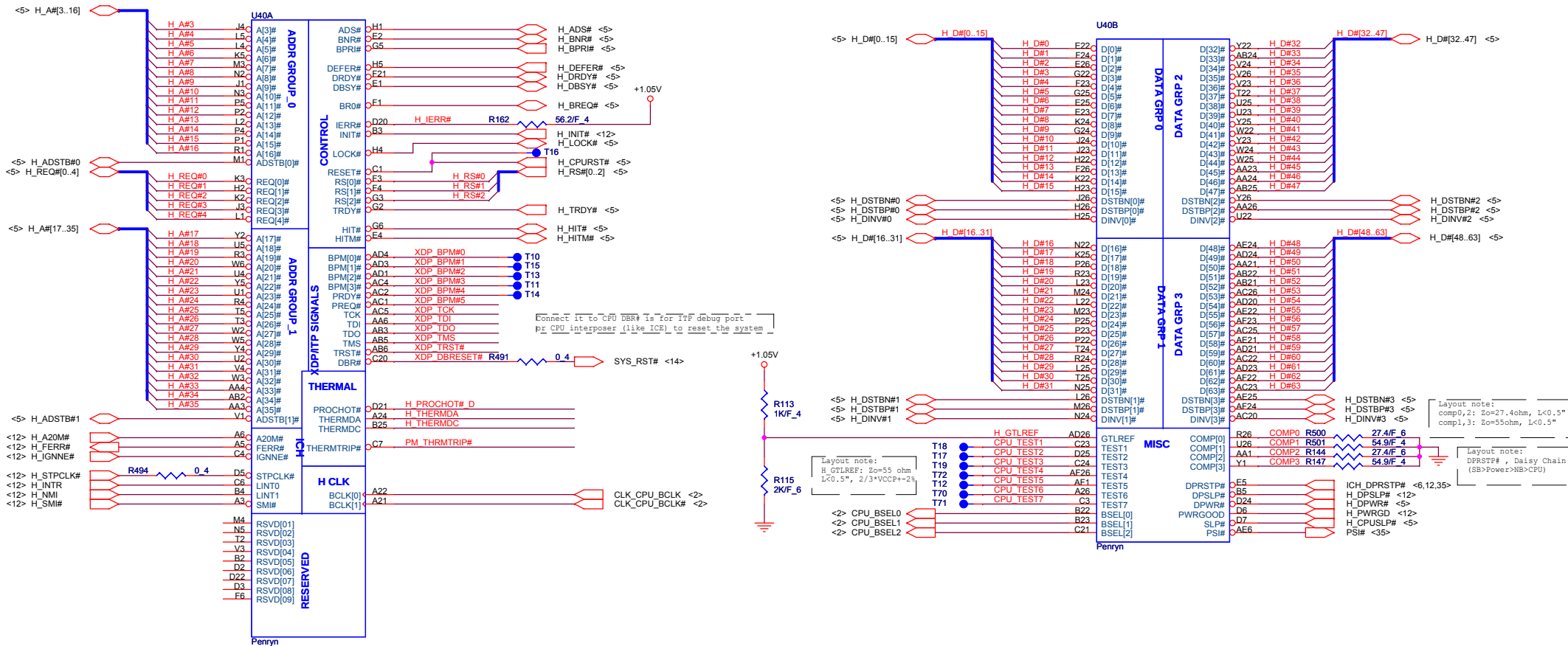
Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS & SRC_0 for external graphic controller support

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

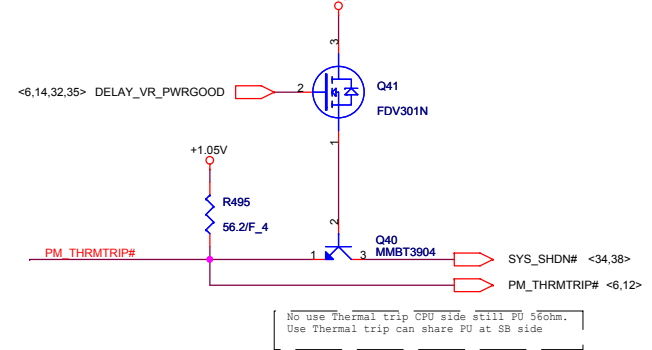


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

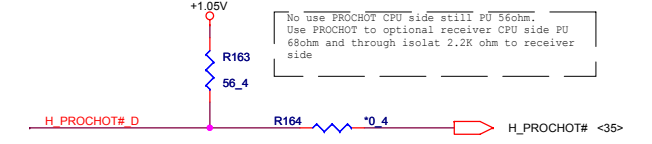
Size	Document Number CLOCK GENERATOR CK505 W/REGULATOR	Rev 1A
Date:	Tuesday, April 08, 2008	Sheet 2 of 40



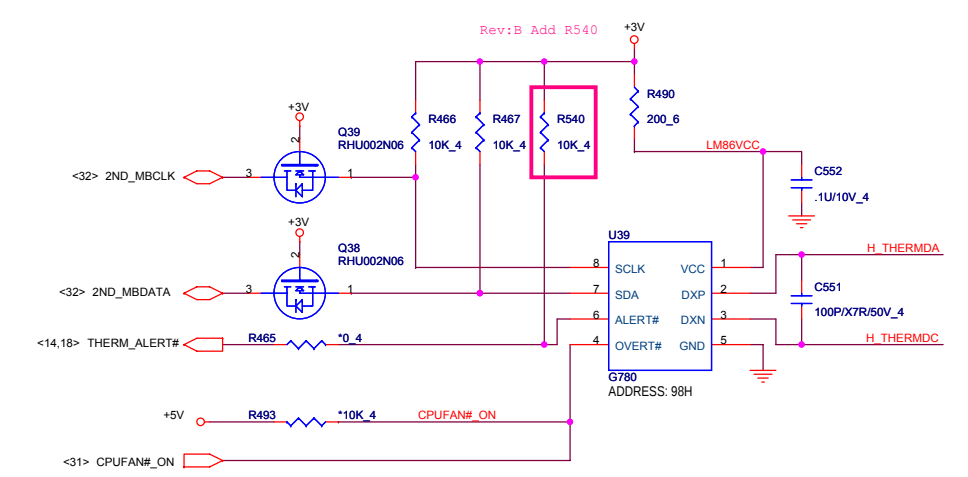
Thermal Trip



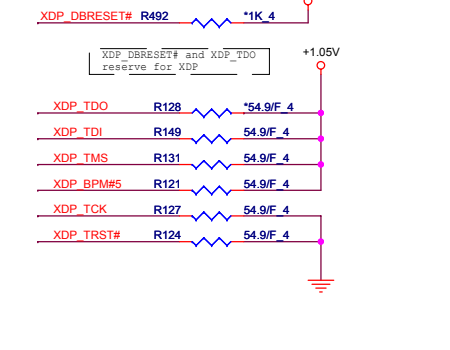
Processor hot

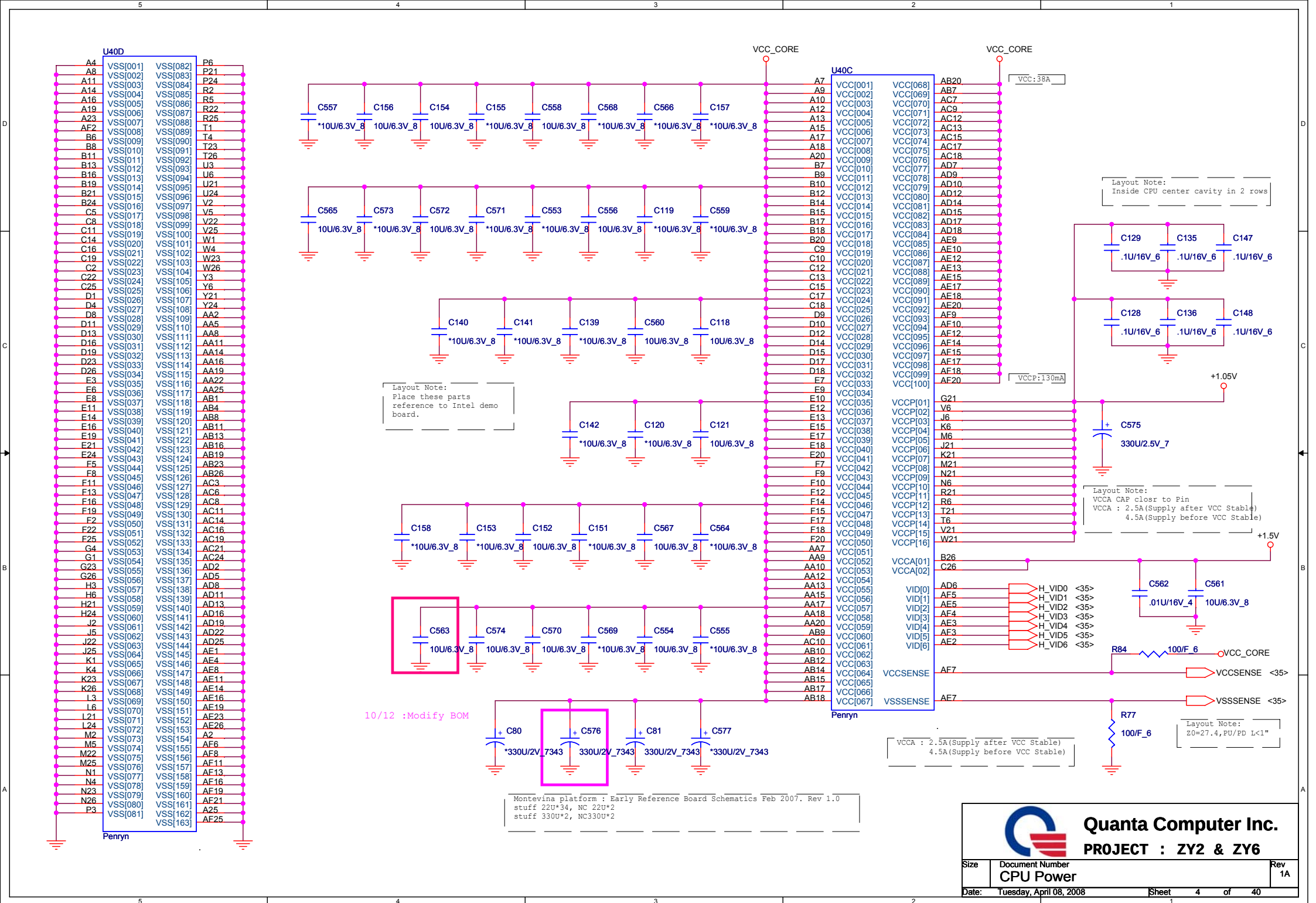


CPU Thermal monitor

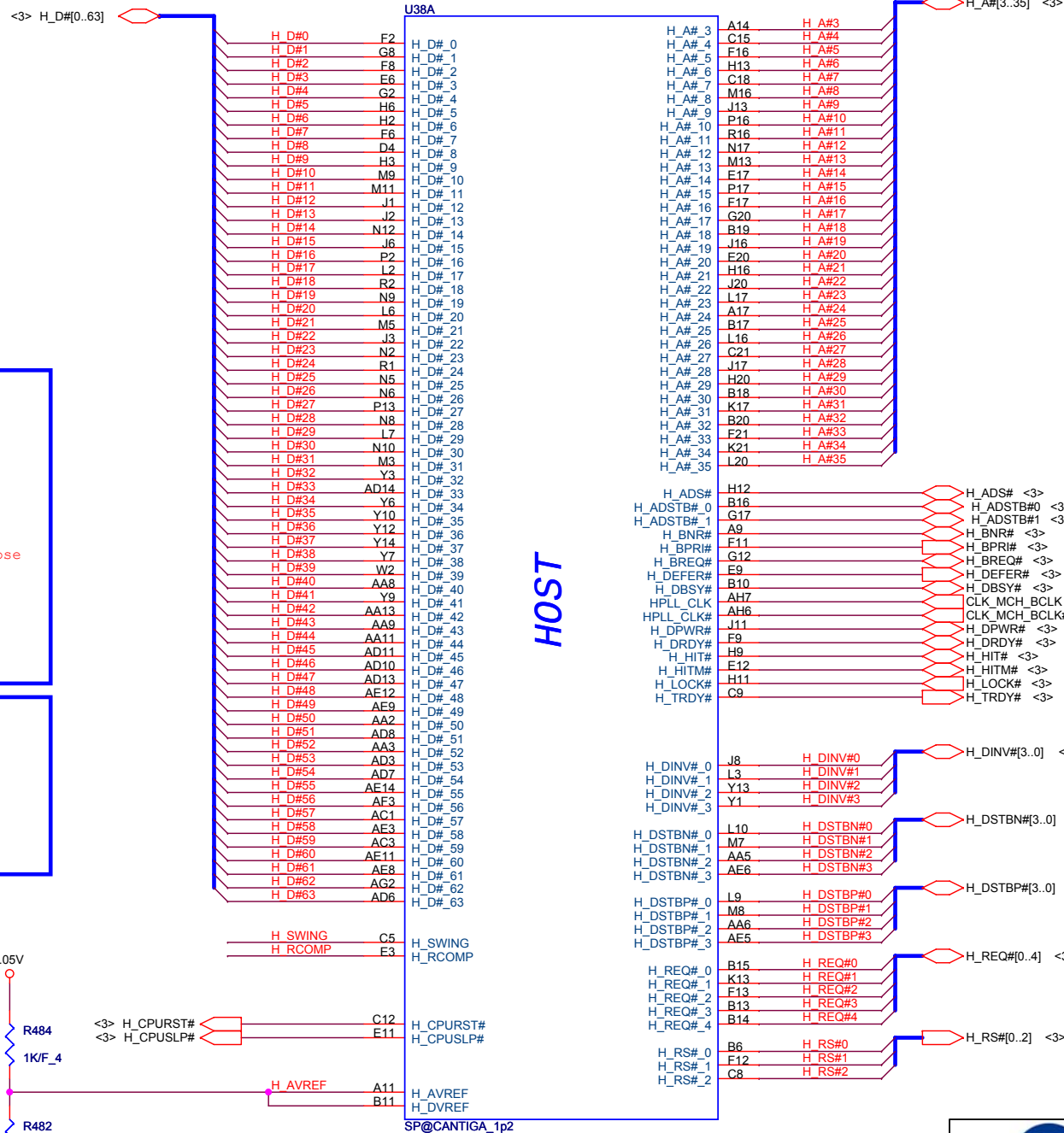
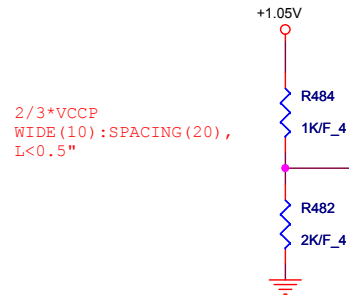
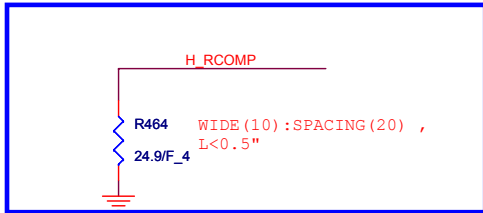
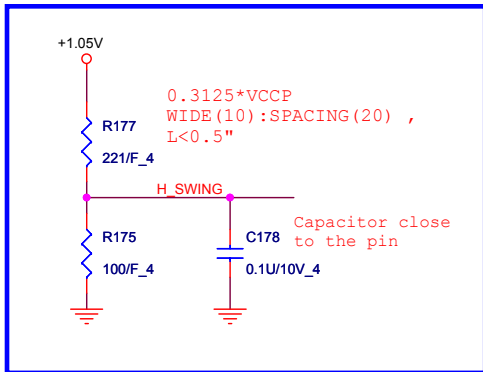


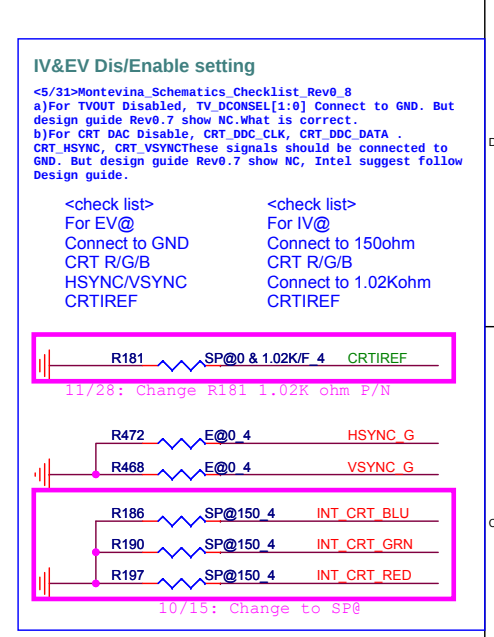
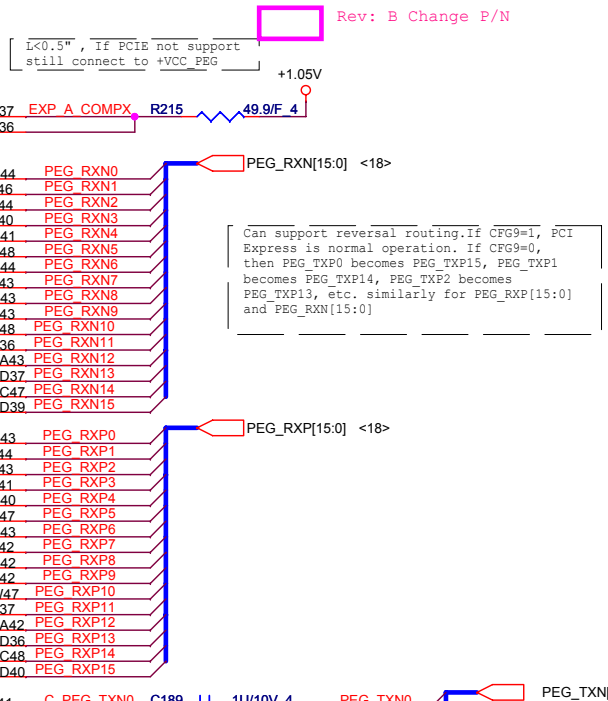
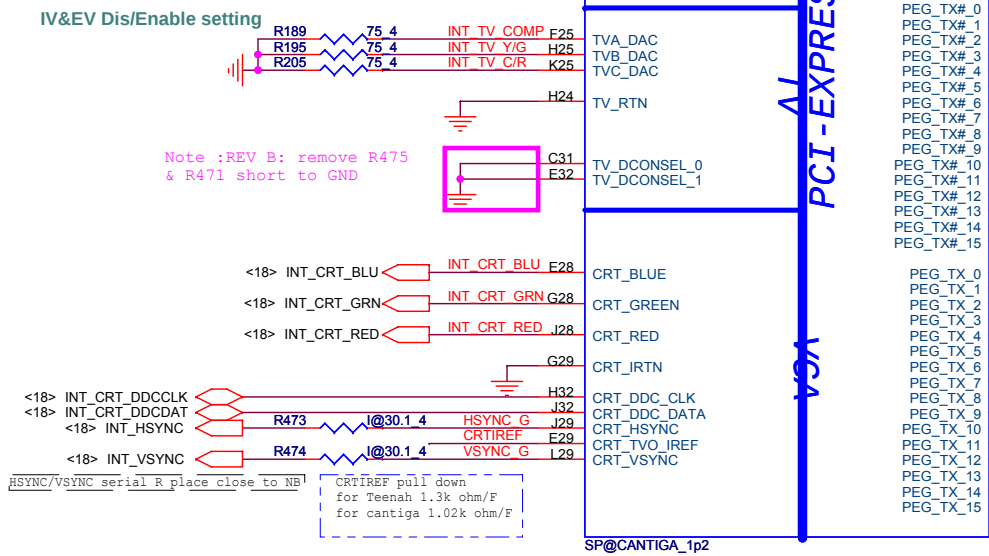
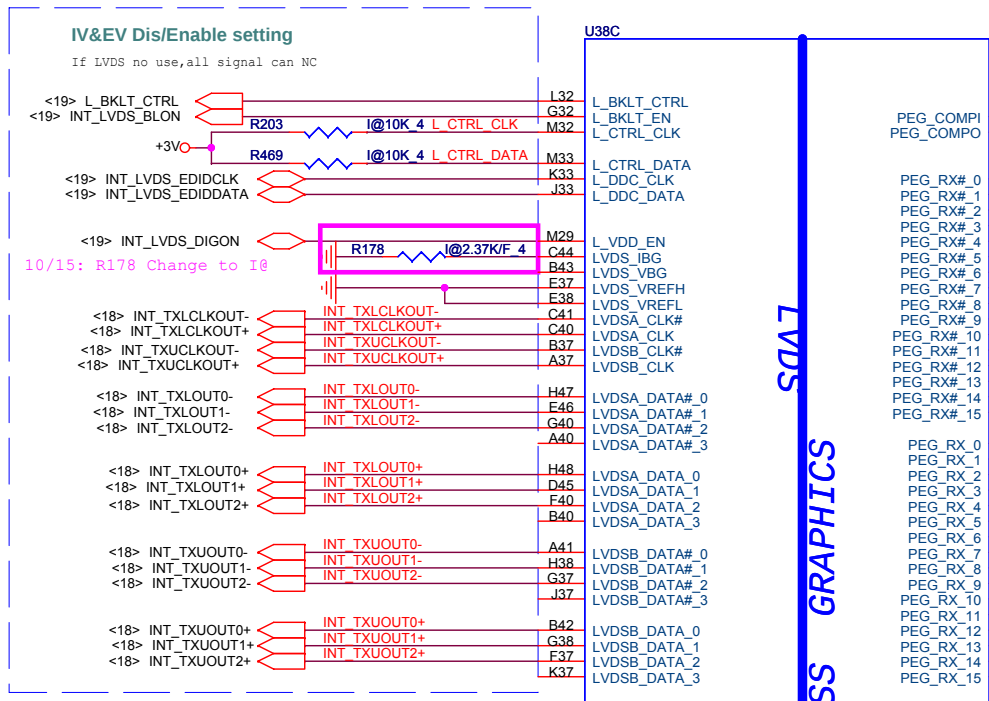
XDP PU/PD

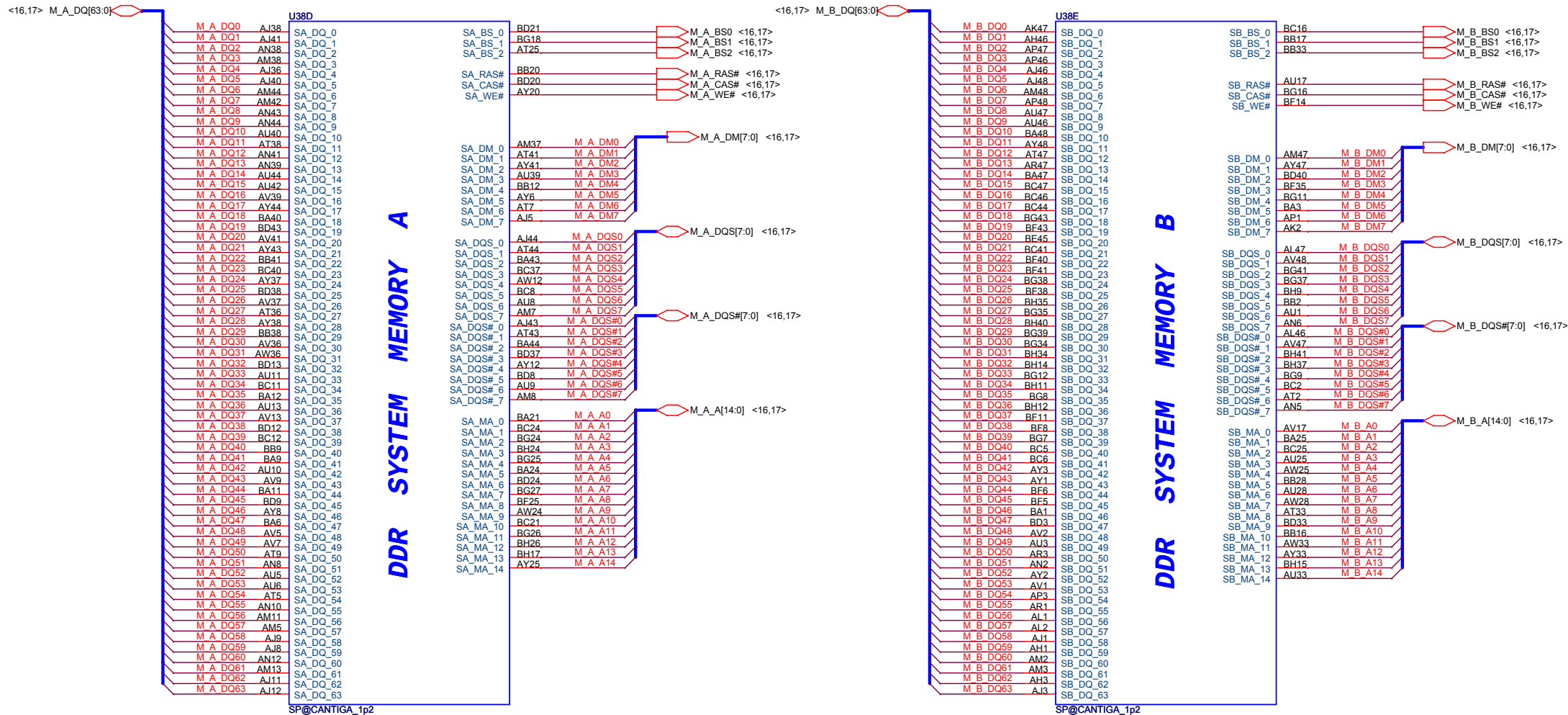




	QCI P/N
Intel Cantiga (G)M	AJ0QT620T01
Intel Cantiga (P)M	AJ0QT780T03







SP@CANTIGA_1p2

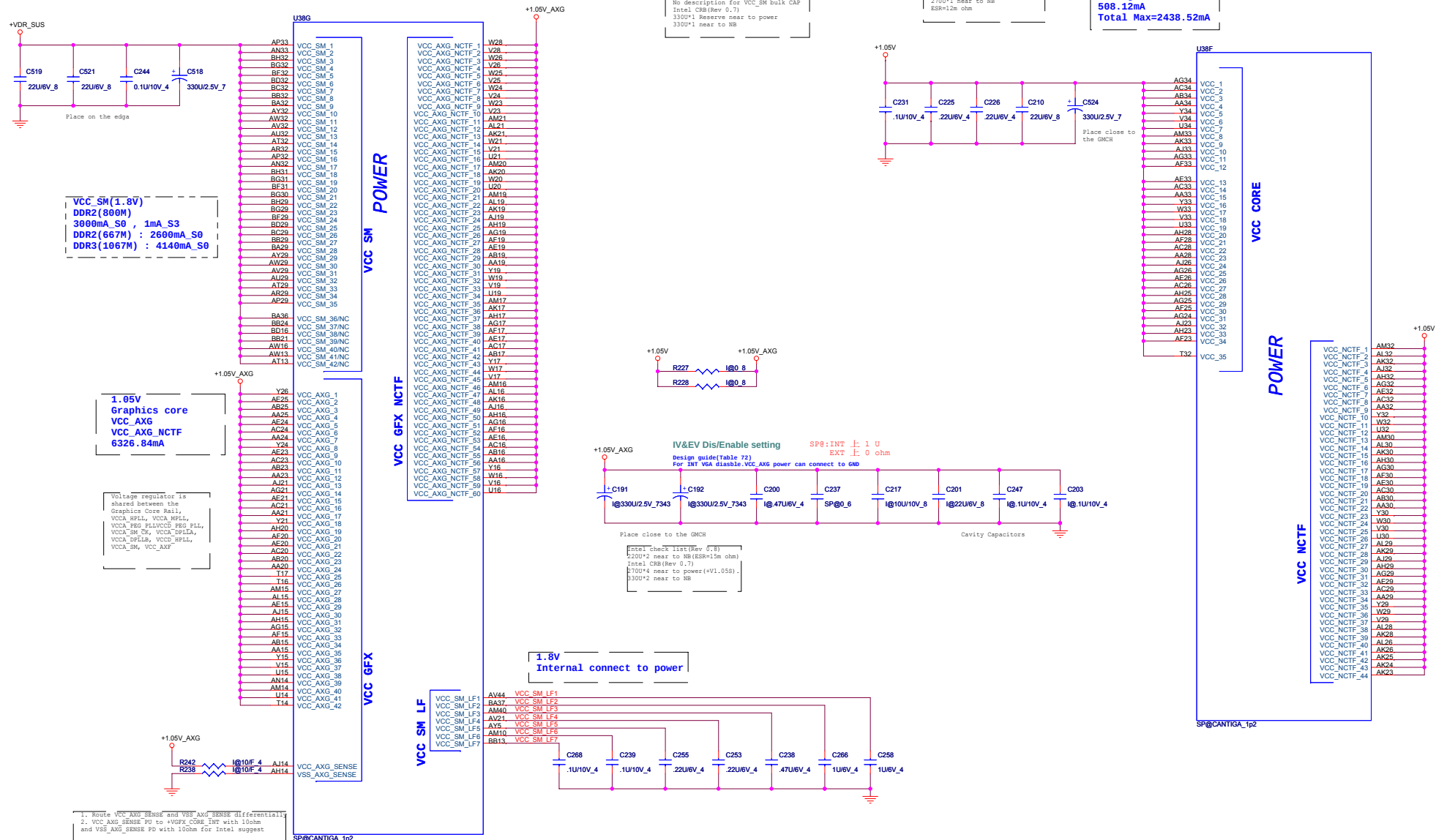
SP@CANTIGA_1p2

GM	TDP	10.5~12W
GS	TDP	7~8W
PM	TDP	7W

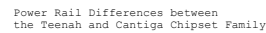
```
Intel check list (Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB (Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm
```

```
VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA
```

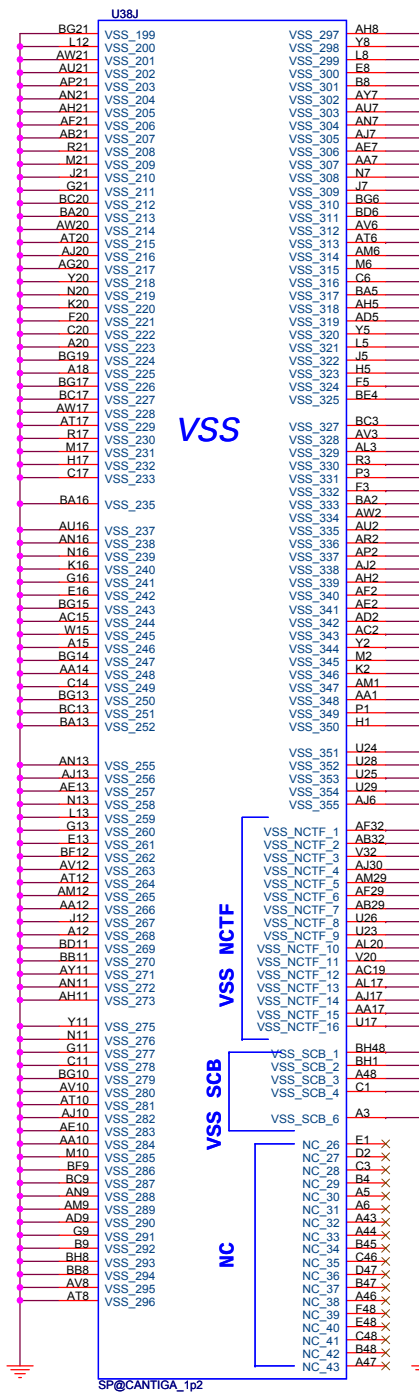
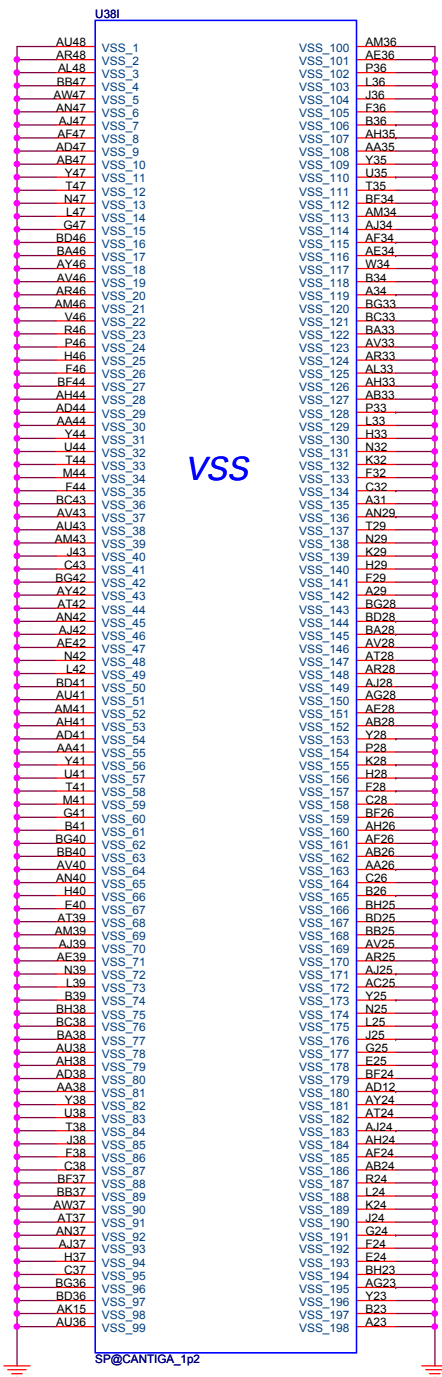
```
Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB
```

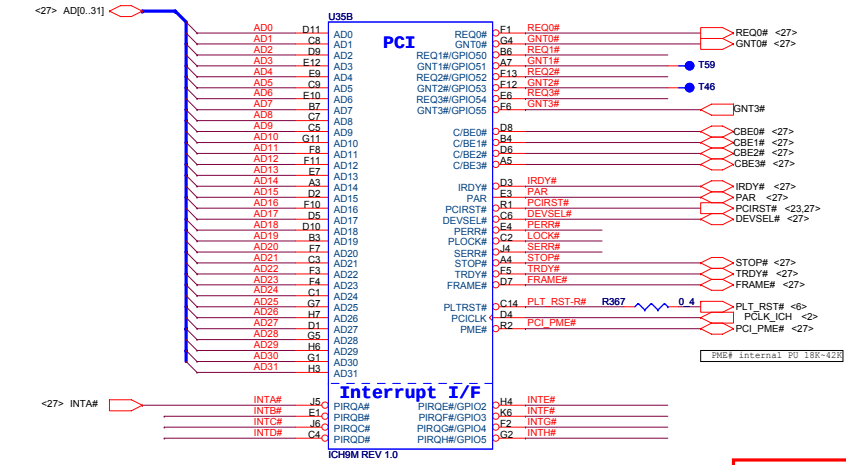


1.05V
FSB-1067
852mA

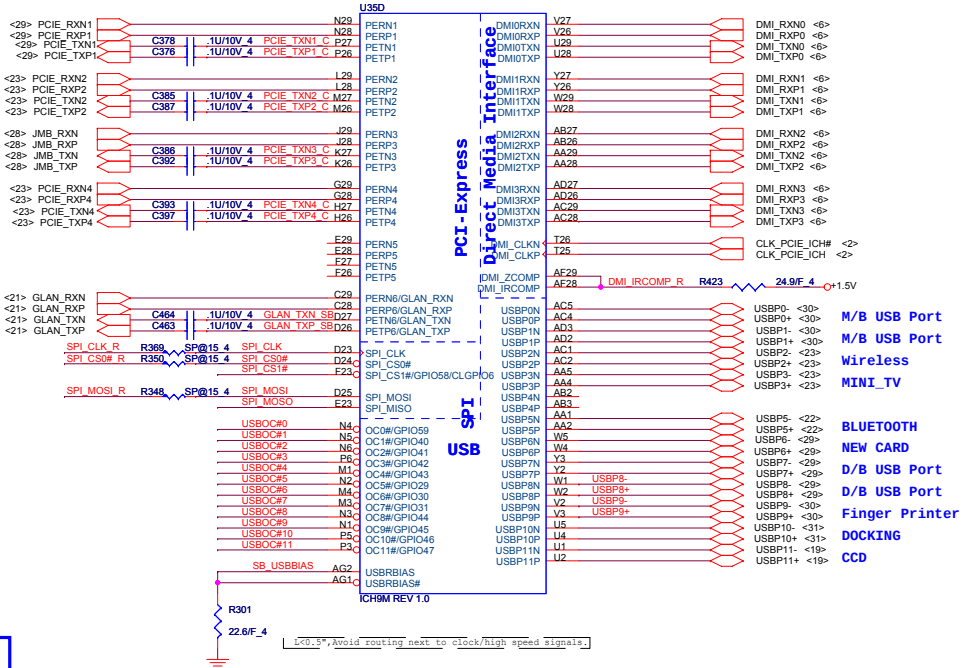
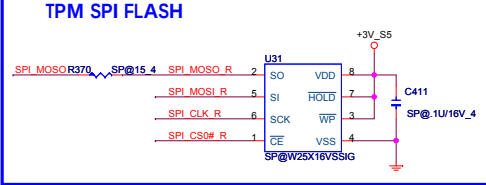
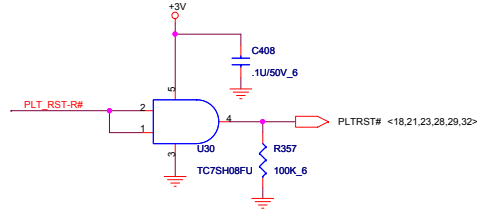


Power Net Name	Cantiga (V)	Tennah (V)	Tennah Current
VCC_AXG # VCC_AXG_NCTF_#	1.05V	1.25V	6326.84mA Cantiga use
VCCA_PEG_BG	1.5V	3.3V	400uA
VCCA_DPLLA	1.05V	1.25V	100mA
VCCA_DPLL	1.05V	1.25V	100mA
VCCA_SM_#	1.05V	1.25V	1065mA
VCCA_HPPLL	1.05V	1.25V	50mA
VCCA_MPLL	1.05V	1.25V	150mA
VCCA_SM_CK_#	1.05V	1.25V	35mA
VCCA_PEG_PLL	1.05V	1.25V	100mA
VCC_AXF_#	1.05V	1.25V	495mA
VCCD_HPPLL	1.05V	1.25V	250mA
VCCD_PEG_PLL	1.05V	1.25V	100mA





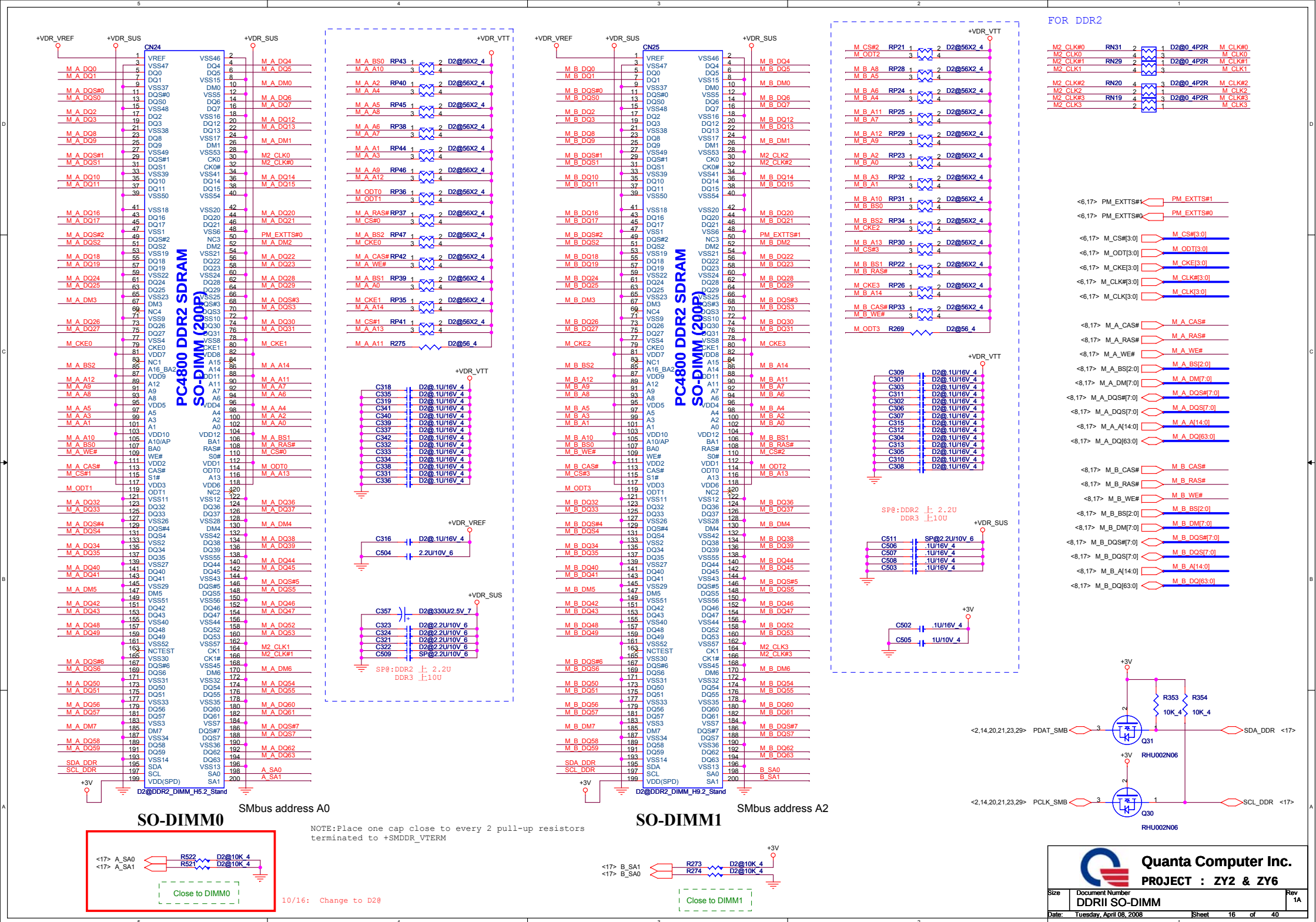
TM & AS	Y
LOW COST	N

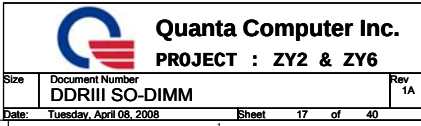


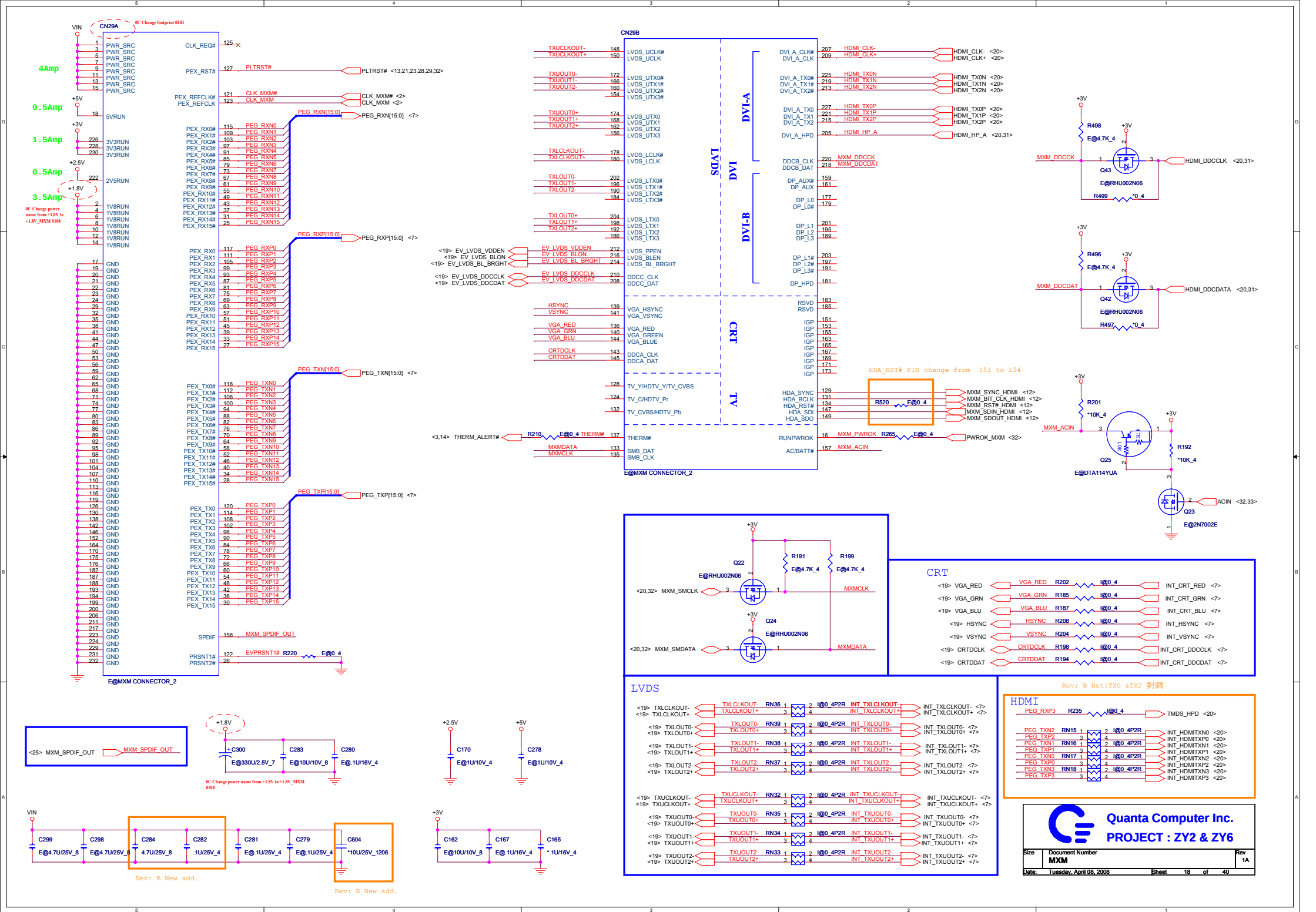
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T

South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD						
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0							
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default							
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default							
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable							
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"><thead><tr><th>PCI_GNT#0</th><th>SPI_CS#1</th><th>Boot Location</th></tr></thead><tbody><tr><td>0</td><td>1</td><td>SPI(Default)</td></tr></tbody></table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI(Default)	
PCI_GNT#0	SPI_CS#1	Boot Location								
0	1	SPI(Default)								
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table border="1"><tbody><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>LPC</td></tr></tbody></table>	1	0	PCI	1	1	LPC	
1	0	PCI								
1	1	LPC								

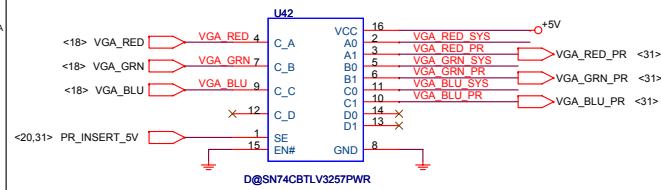




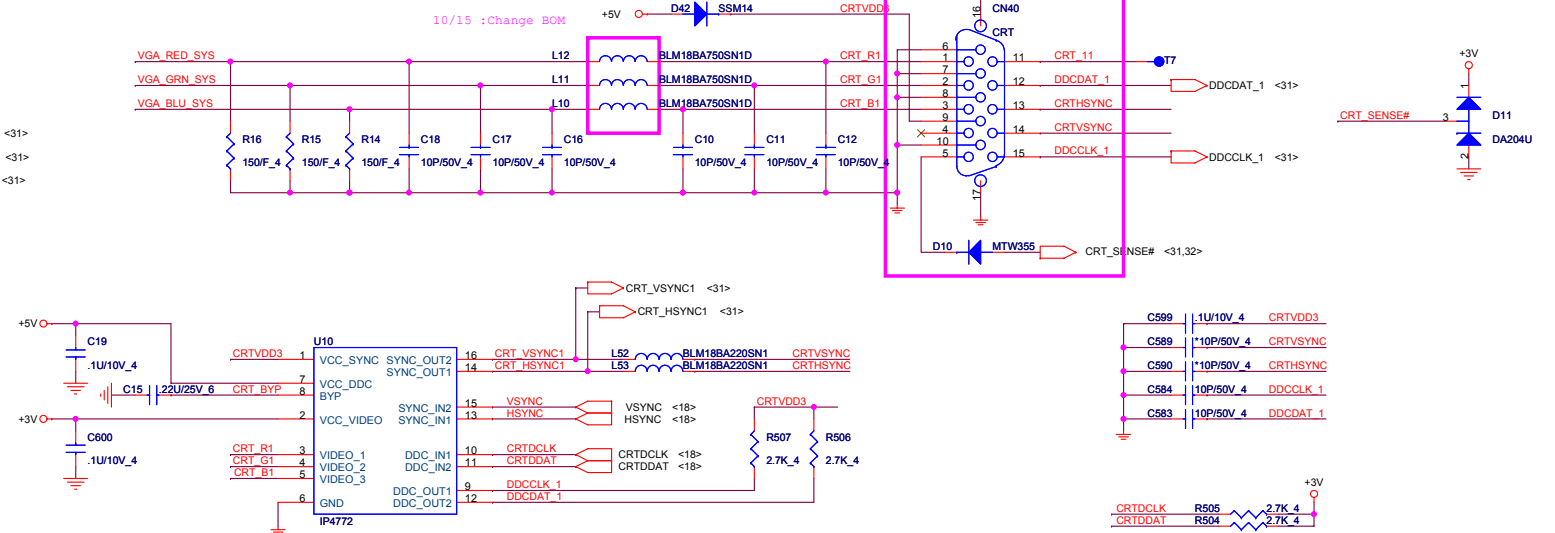


CRT Select

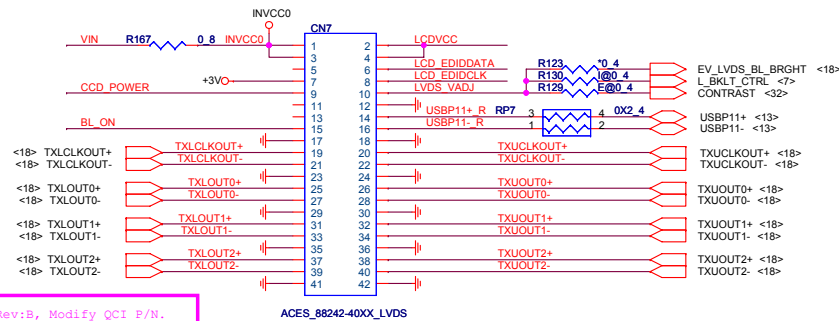
CRT SWITCH



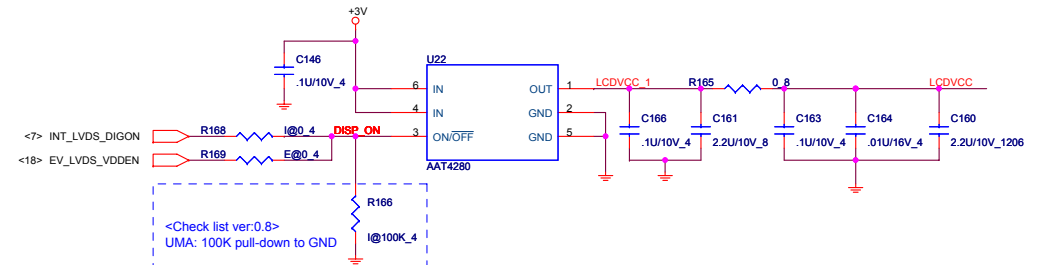
CRT CONNECTOR AND ESD



LVDS



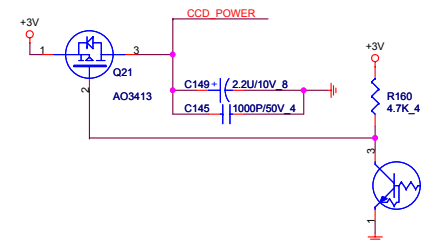
Rev:B, Modify QCI P/N.



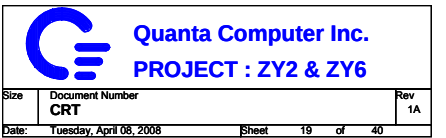
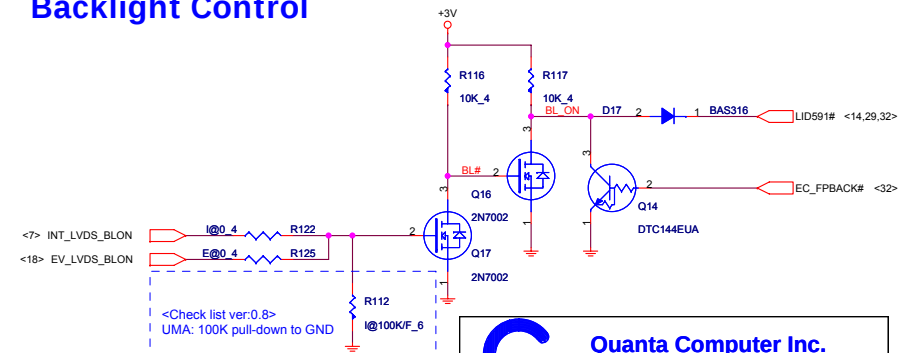
Rev:C, Change to 4.7U 0805



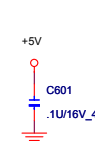
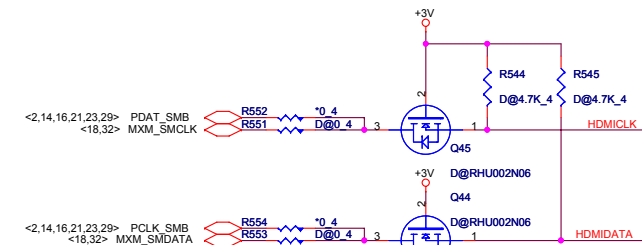
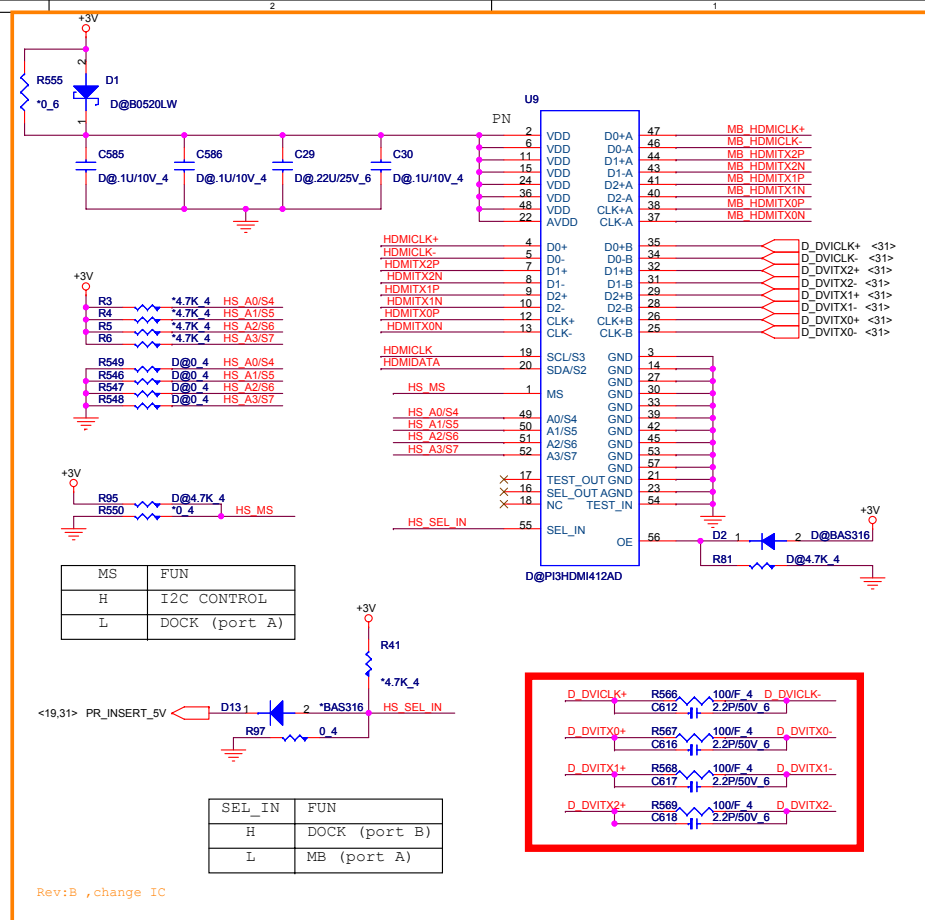
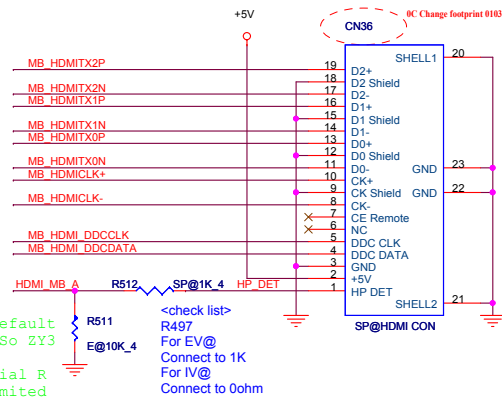
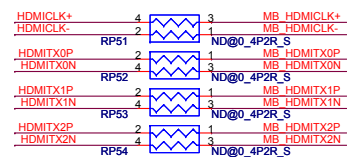
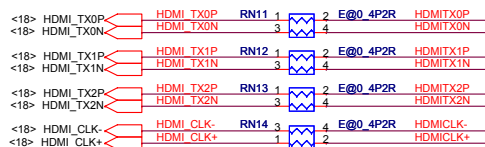
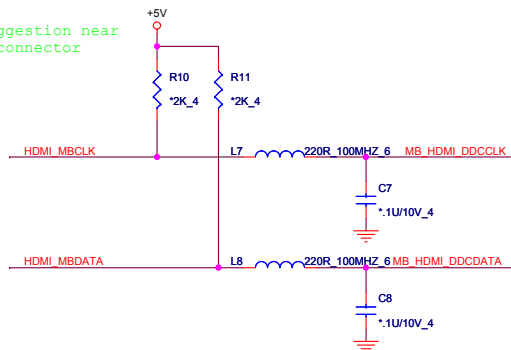
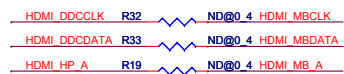
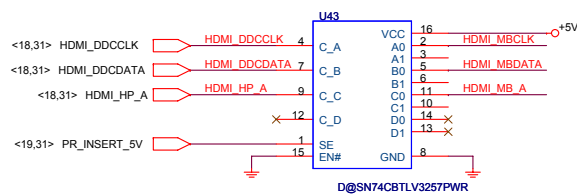
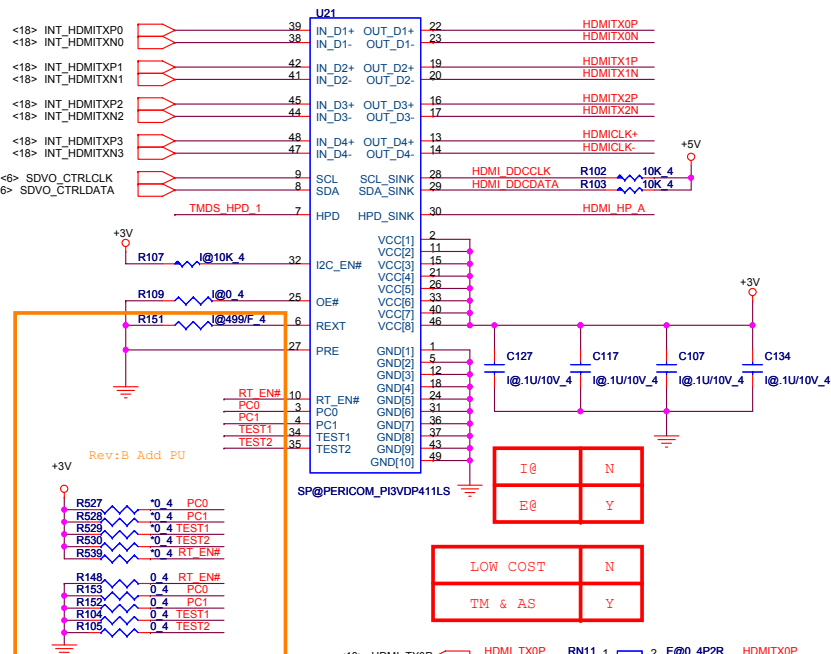
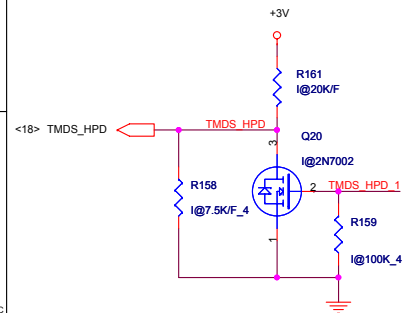
CAMERA MODULE CONNECTOR



Backlight Control



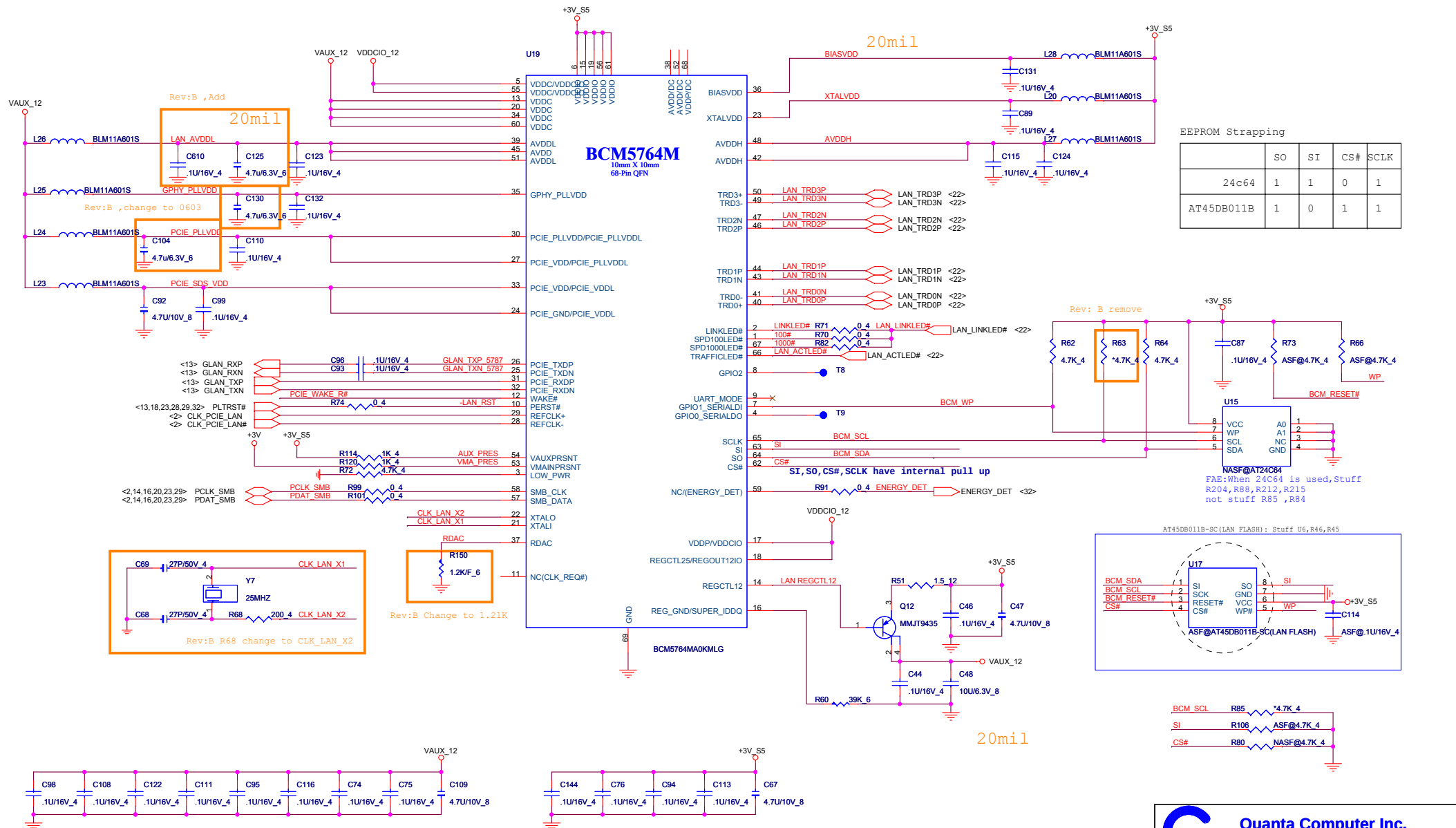
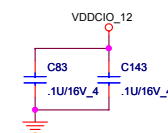
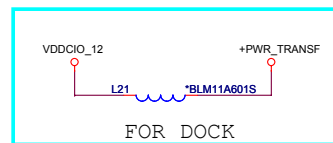
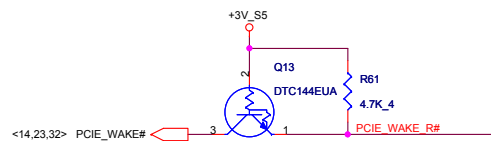
	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



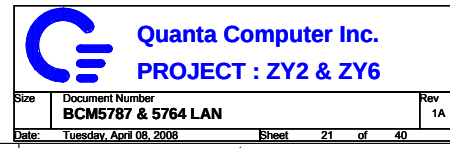
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number LVDS/HDMI/CAMERA/LID	Rev 1A
Date:	Wednesday, April 09, 2008	Sheet 20 of 40

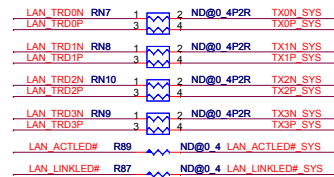
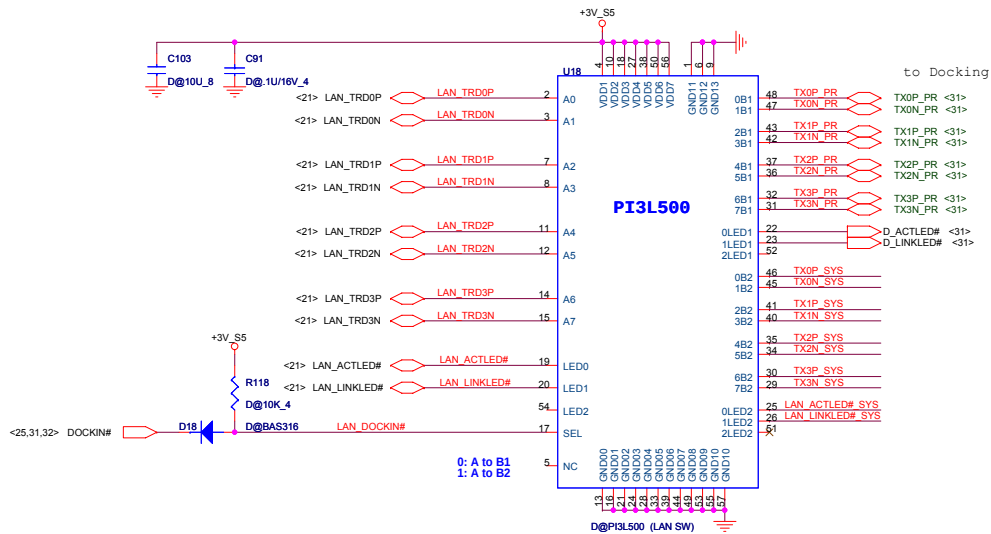
LAN



Low is normal, H->Turn Off 1.2V,
H(>0.7V <2.5V)->L will internal
reset

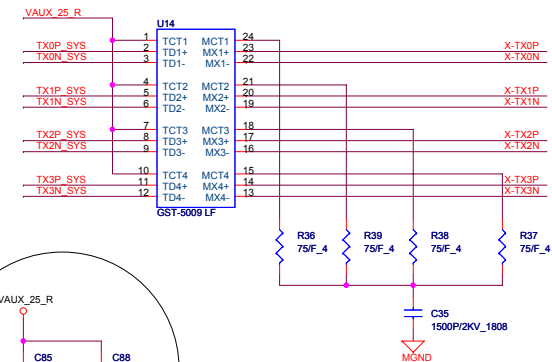


LAN SWITCH

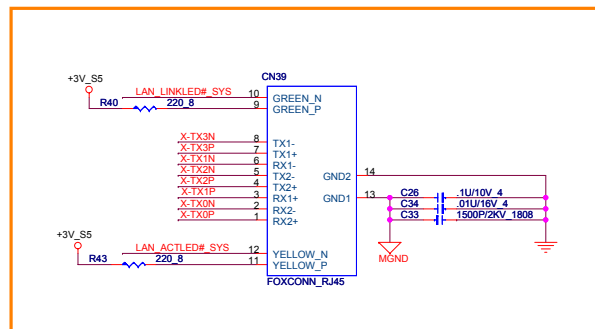


Transformer

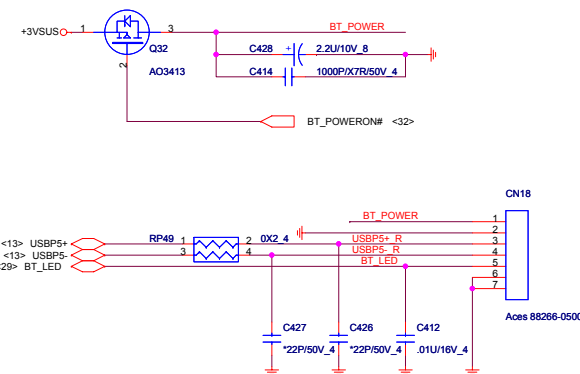
Source 1: DELTA LFE9249 DB0ZR1LAN11
Source 2: Bothand GST5009 DBKN1NLAN03



RJ45-11

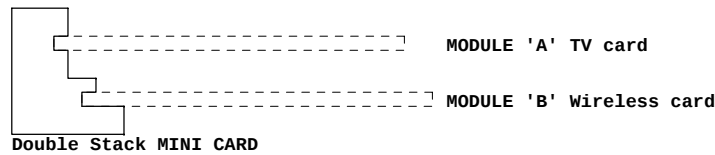


BLUETOOTH MODULE CONNECTOR

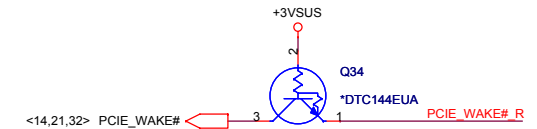
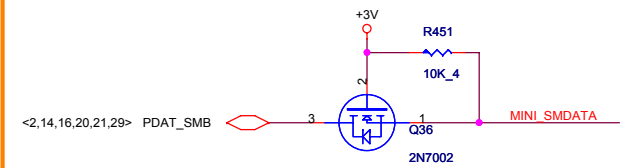
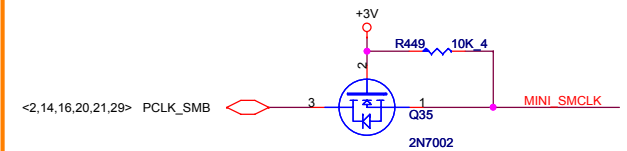
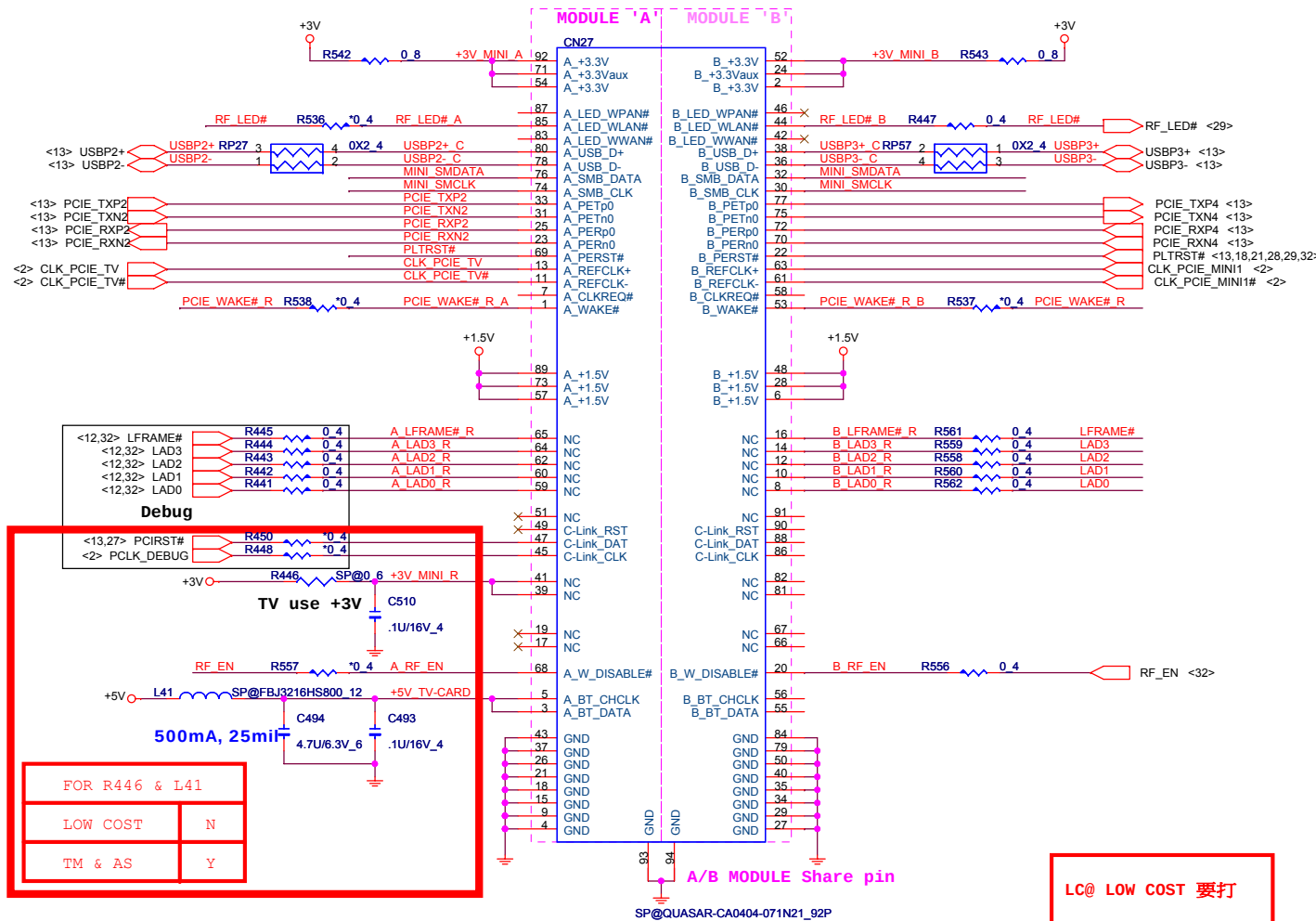


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

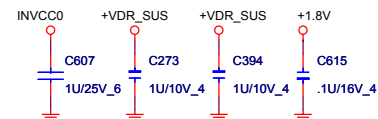
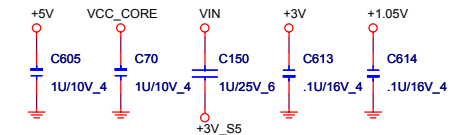
MINI-CARD



Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538

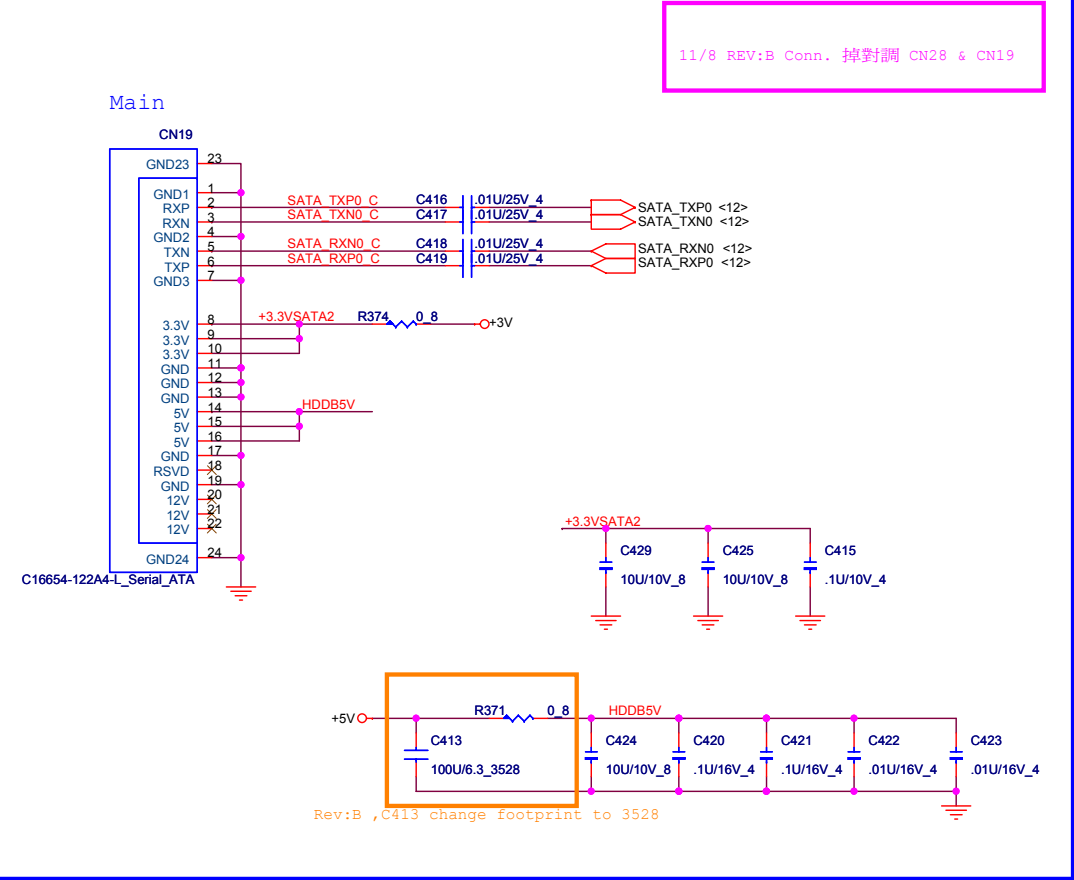


FOR EMI

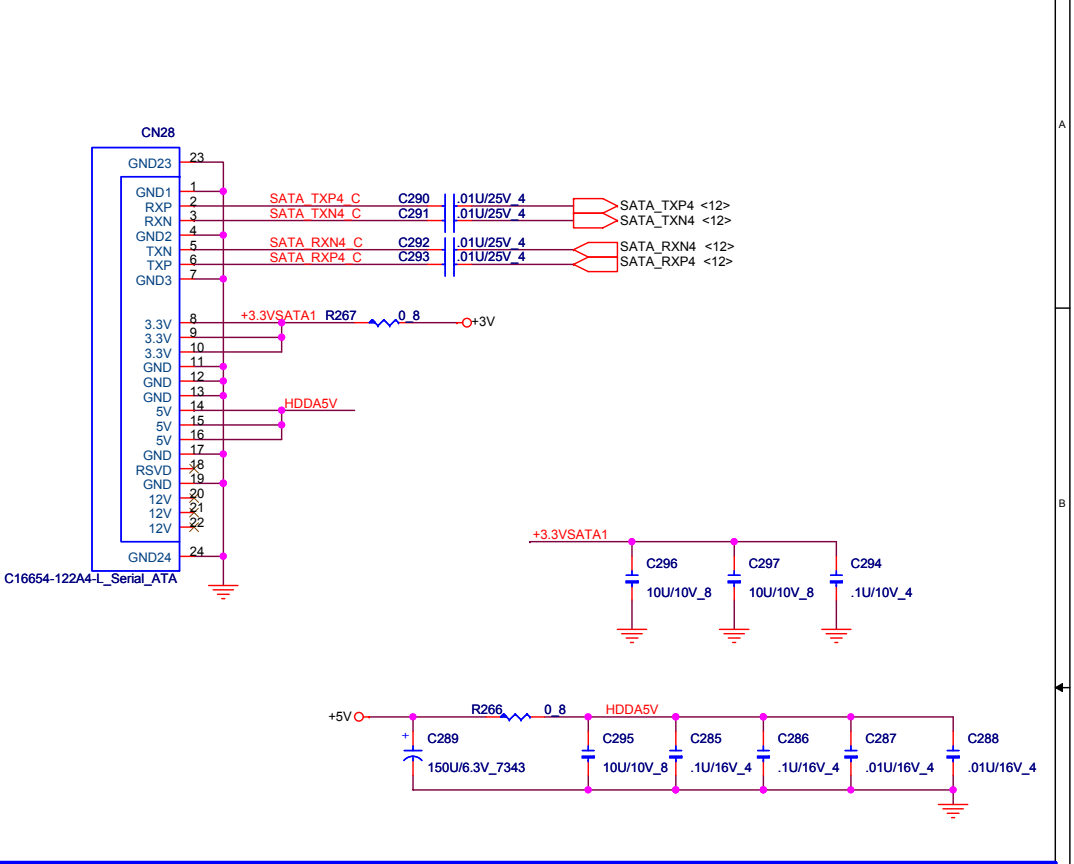


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

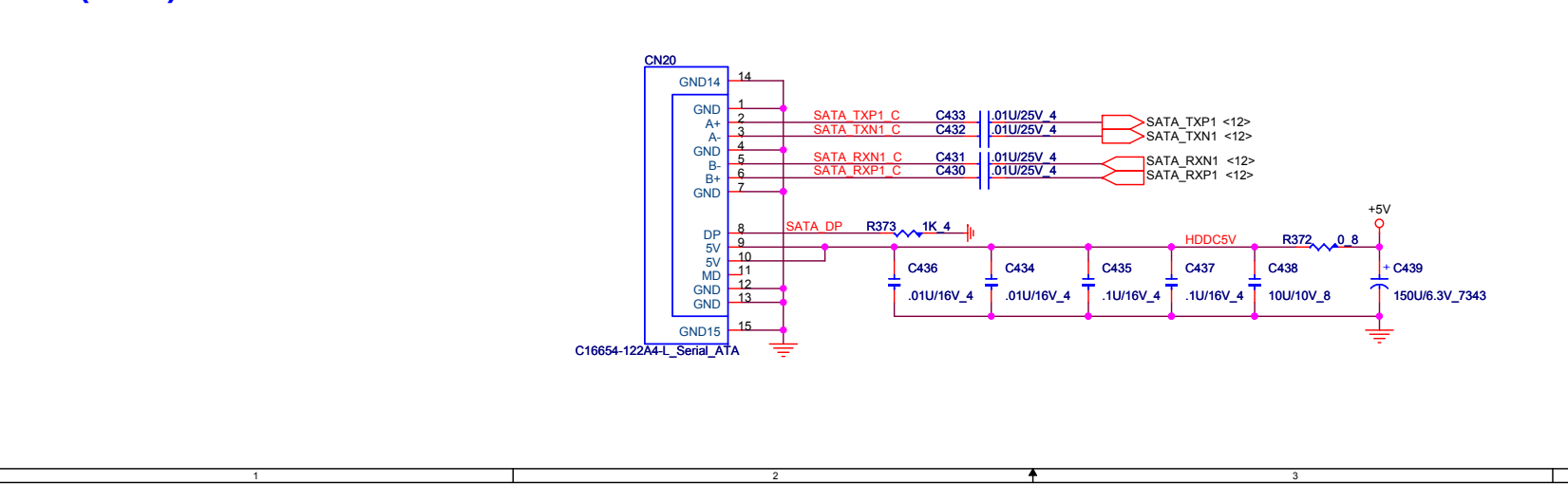
SATA HDD



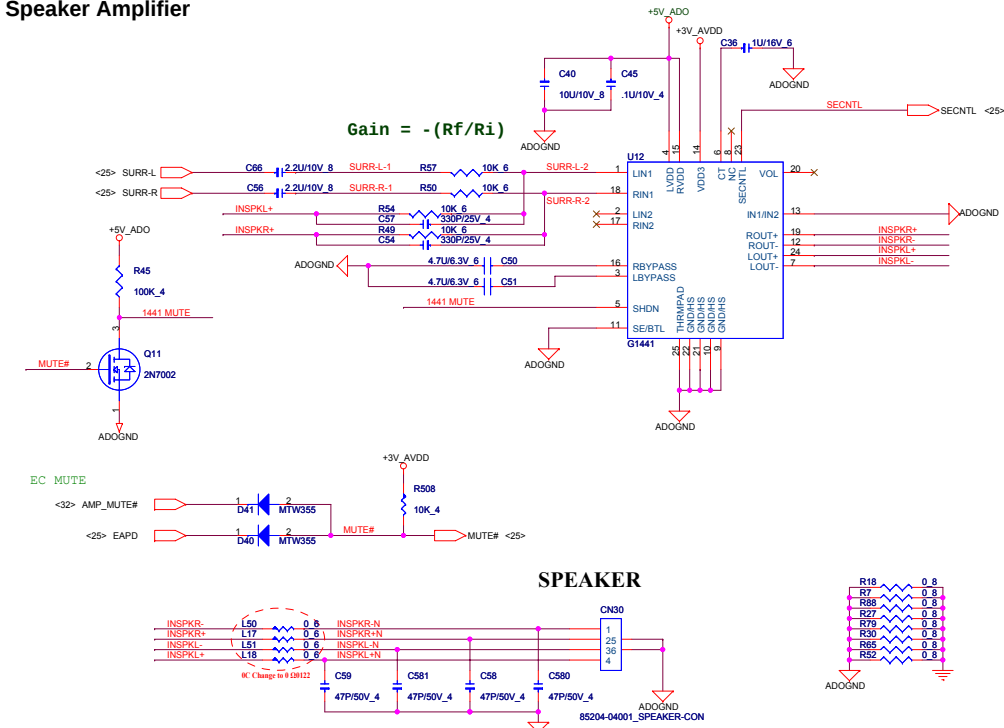
2ND SATA HDD



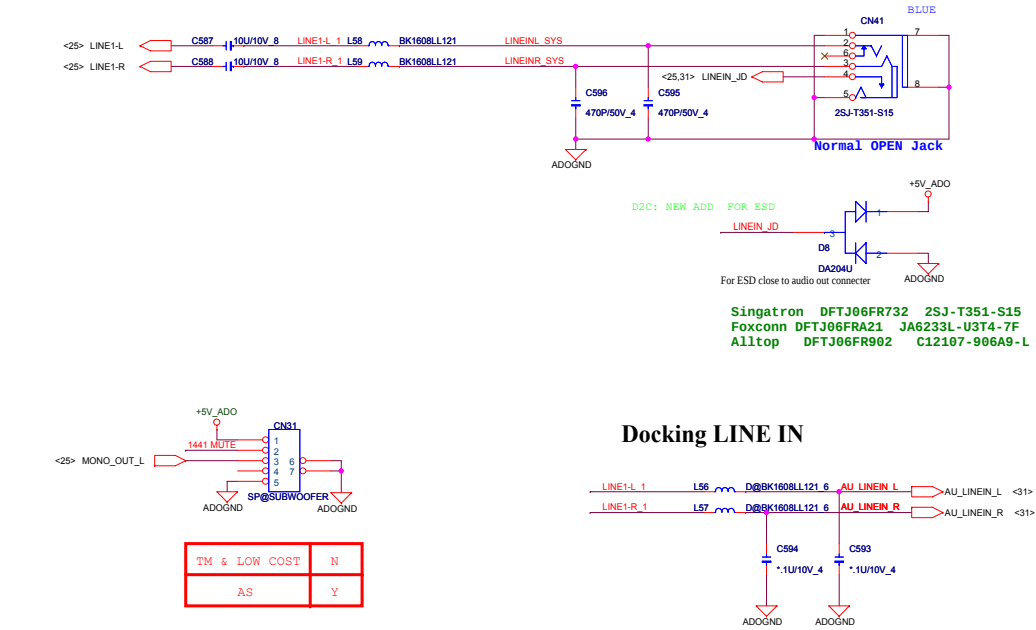
ODD (SATA)



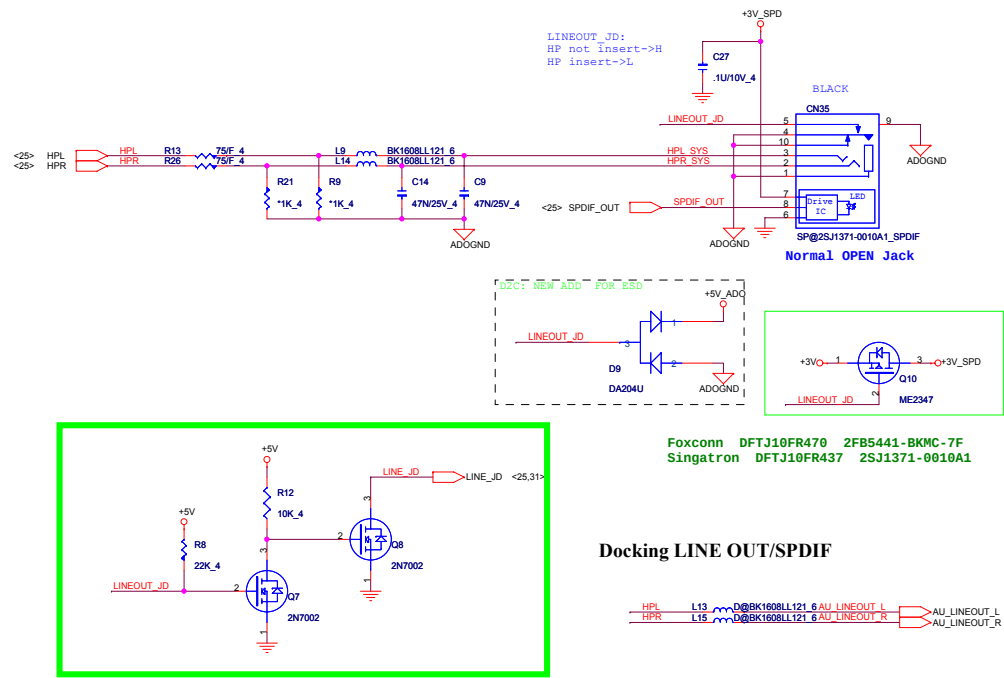
Speaker Amplifier



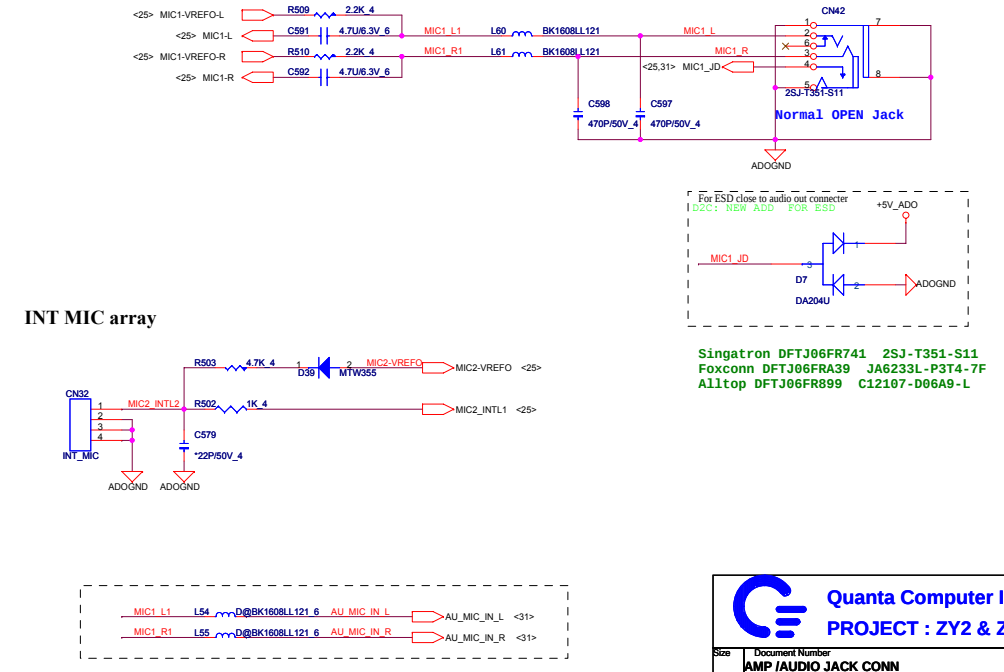
SYSTEM LINE IN/SUBWOOFER



SYSTEM LINE OUT/SPDIF



MIC



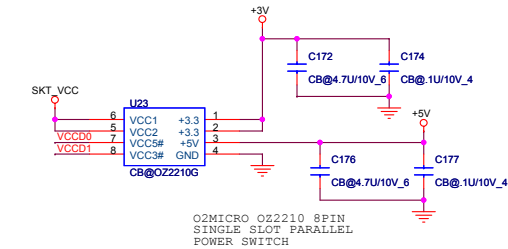
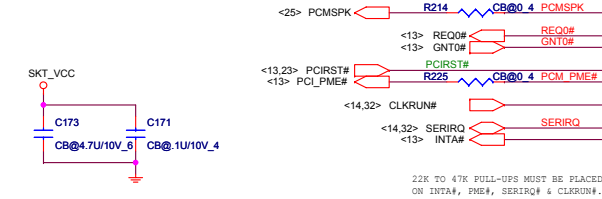
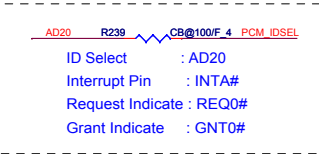
NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

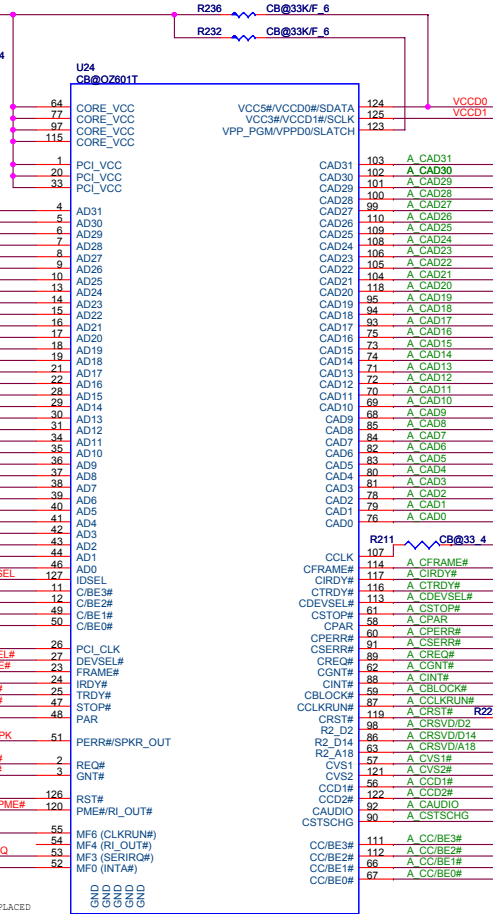
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

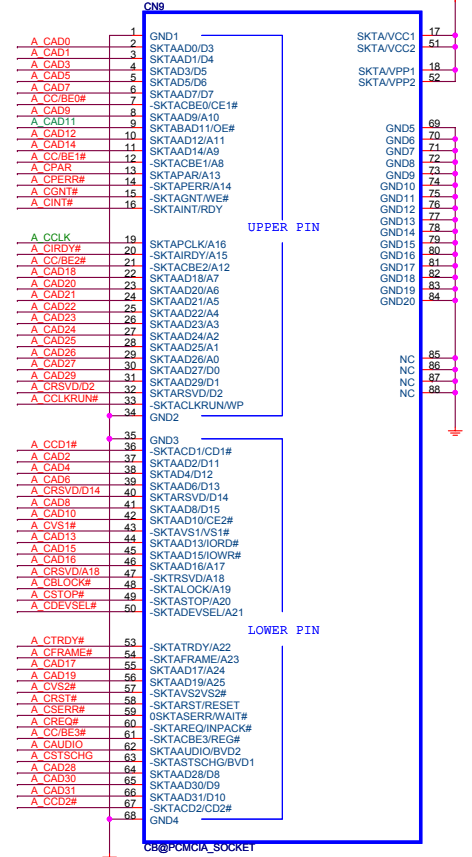
VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127



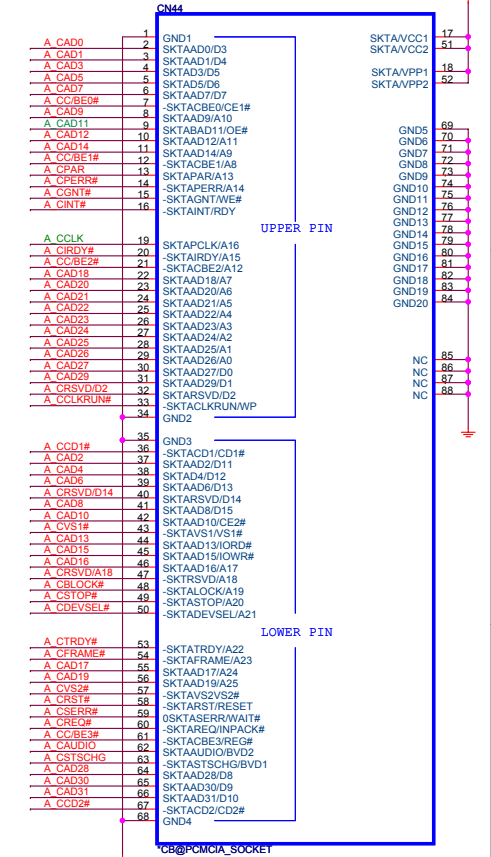
IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



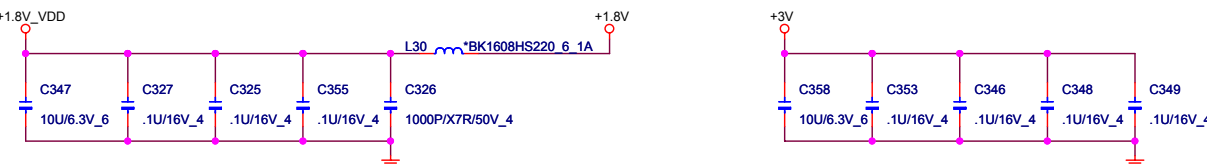
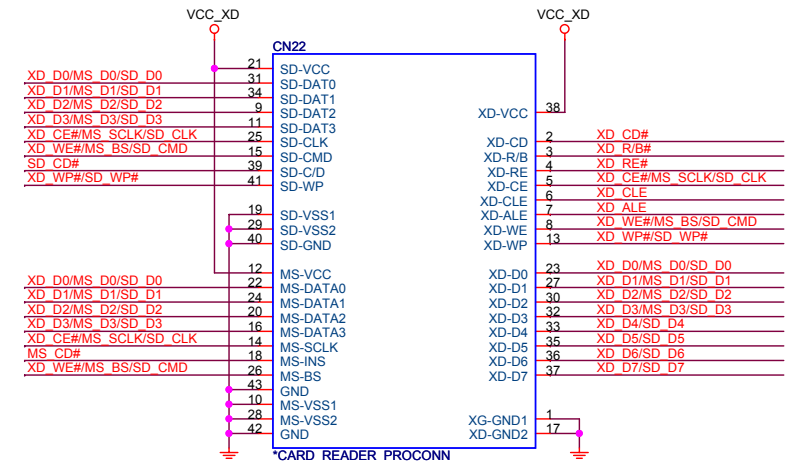
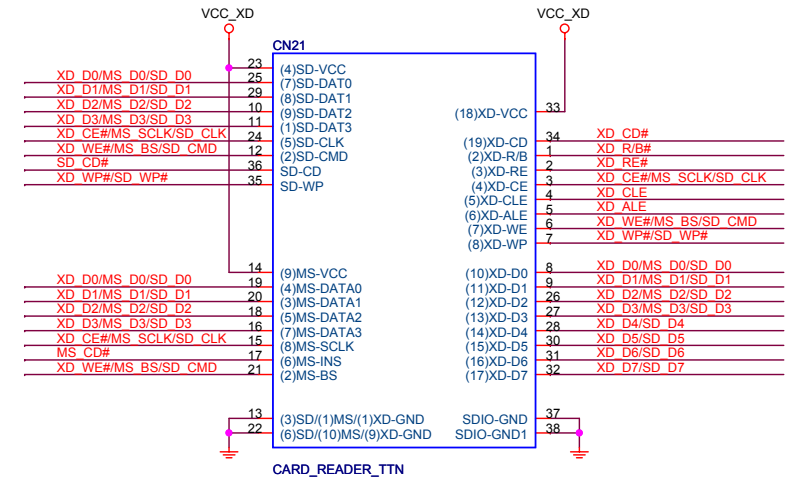
PCMCIA SOCKET



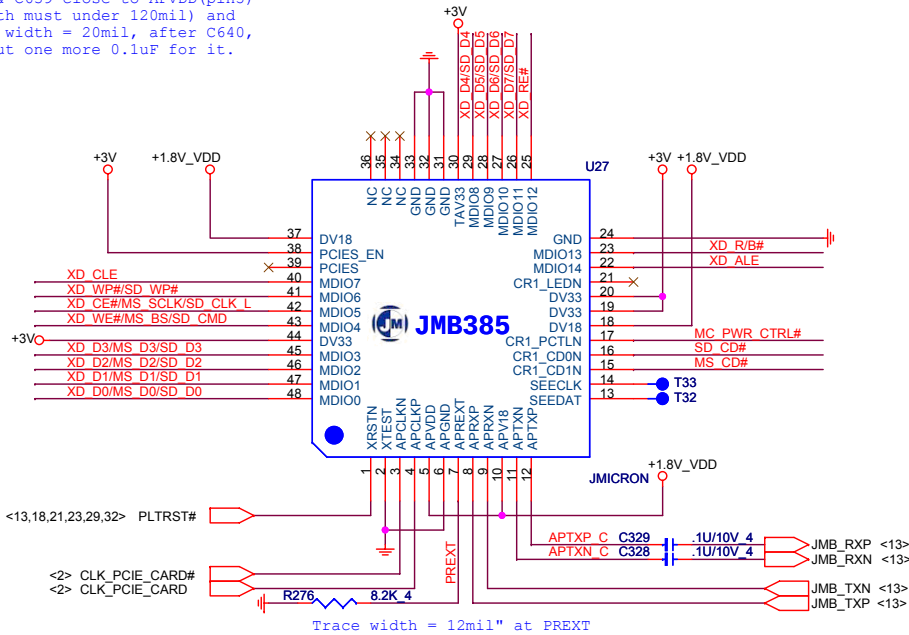
PCMCIA SOCKET



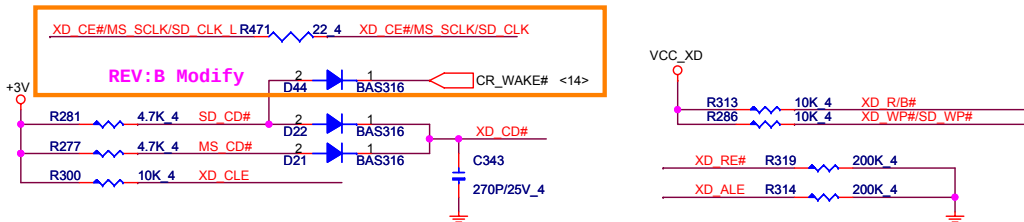
7 IN 1 CARD READER



C640 & C639 close to APVDD(pin5)
(length must under 120mil) and
trace width = 20mil, after C640,
pls put one more 0.1uF for it.

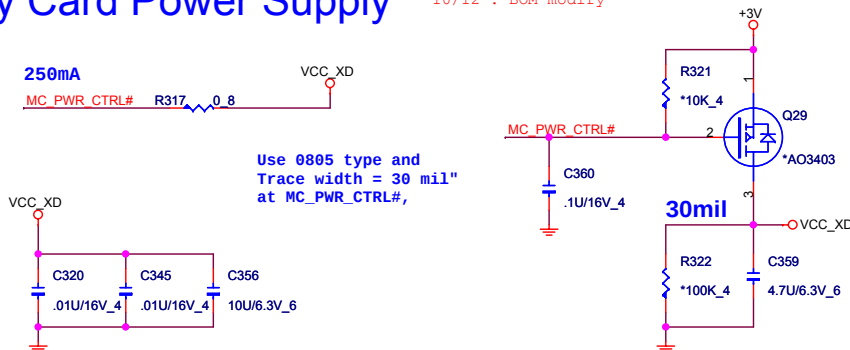


Rev: B Add. for Vendor request



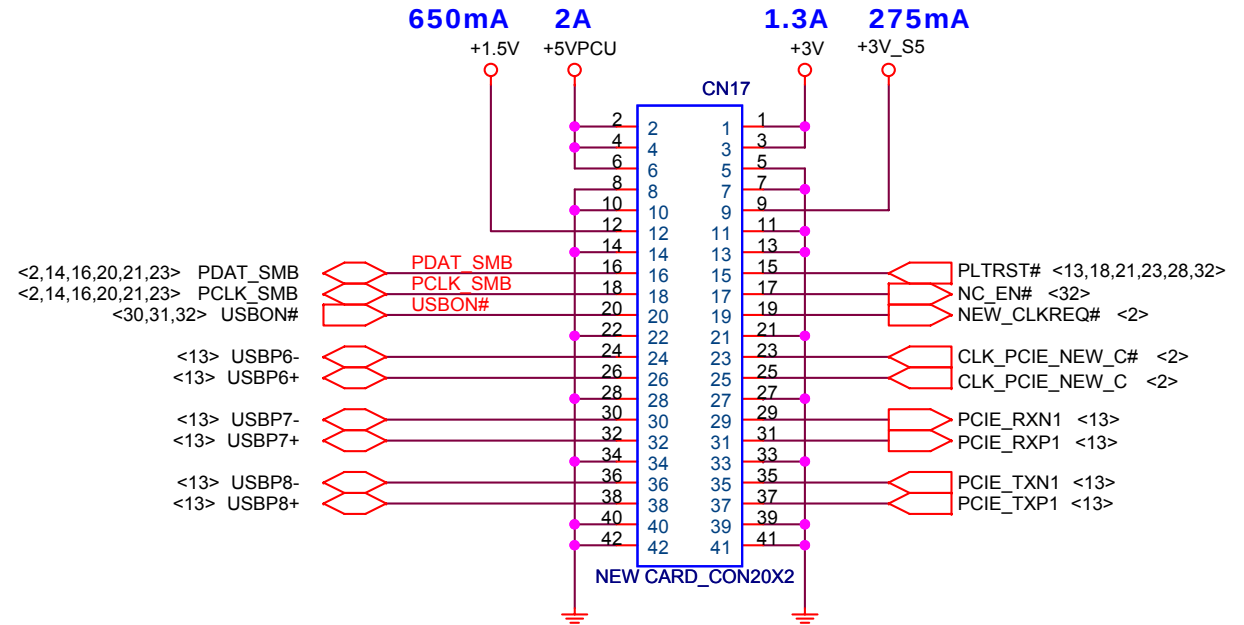
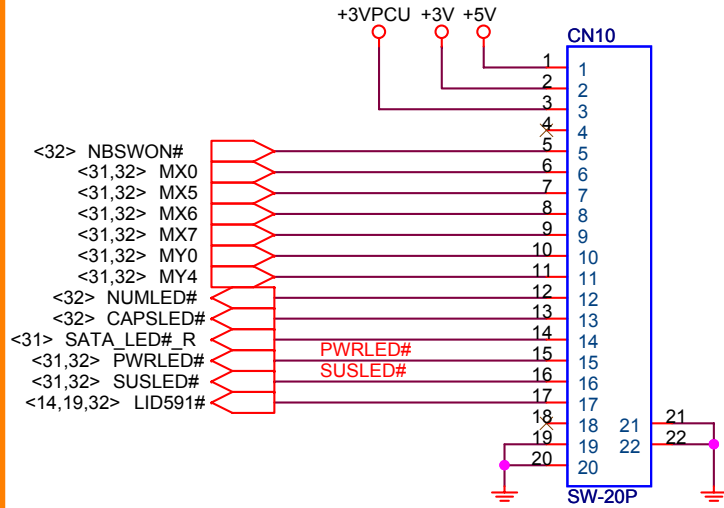
Memory Card Power Supply

10/12 : BOM modify

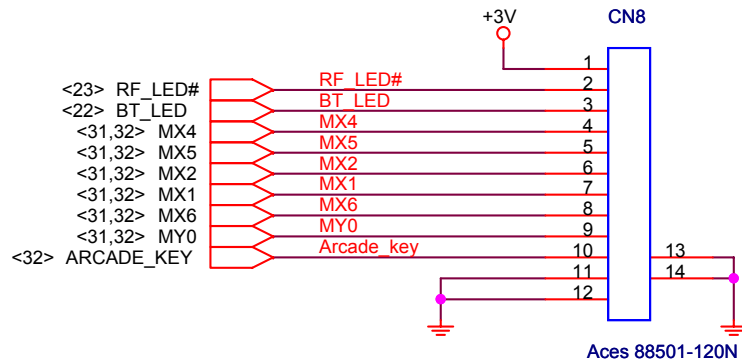


To NEW-CARD & EXT. USB

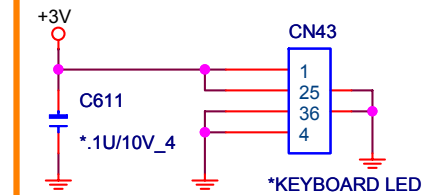
REV:B, CN10 change footprint



REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Fncion	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4



Rev:B Add CN43 For backlight KB

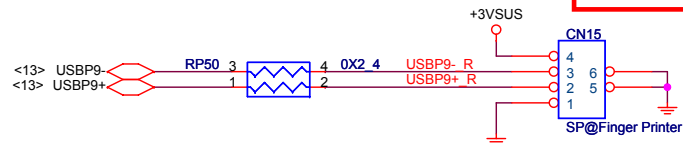
Rev:B Change to 圖 to 方PAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395



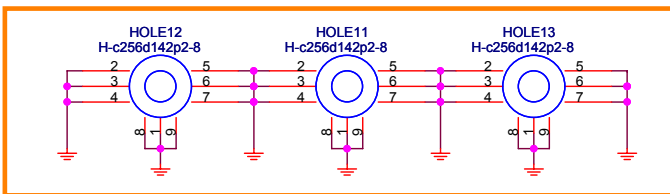
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Finger Printer

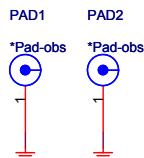
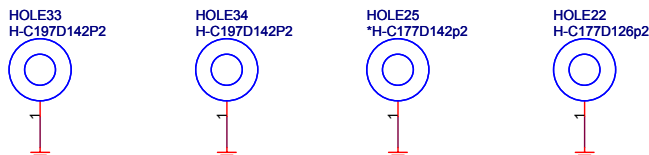
TM & AS	Y
LOW COST	N



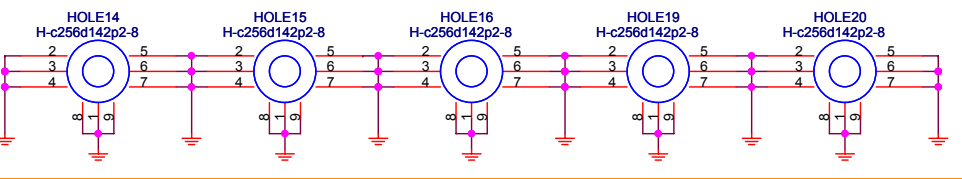
HOLES CPU NUT (BOT)



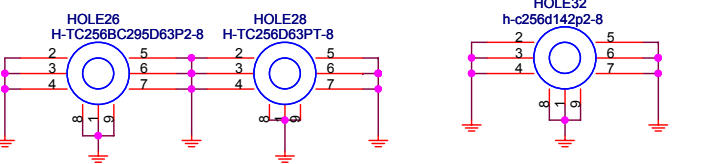
Rev : B Add MINI NUT



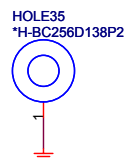
MXM NUT (BOT)



MDC NUT (TOP)

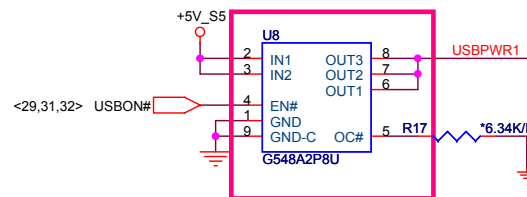


Rev:B New add HOLE32
HOLE26 & 28 Change footprint

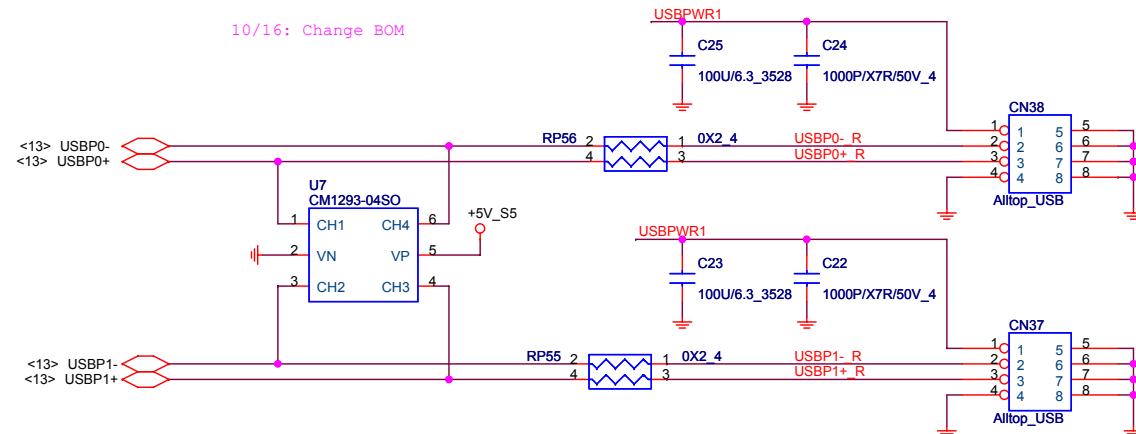


HOLE35 要搬到BOT去

USB

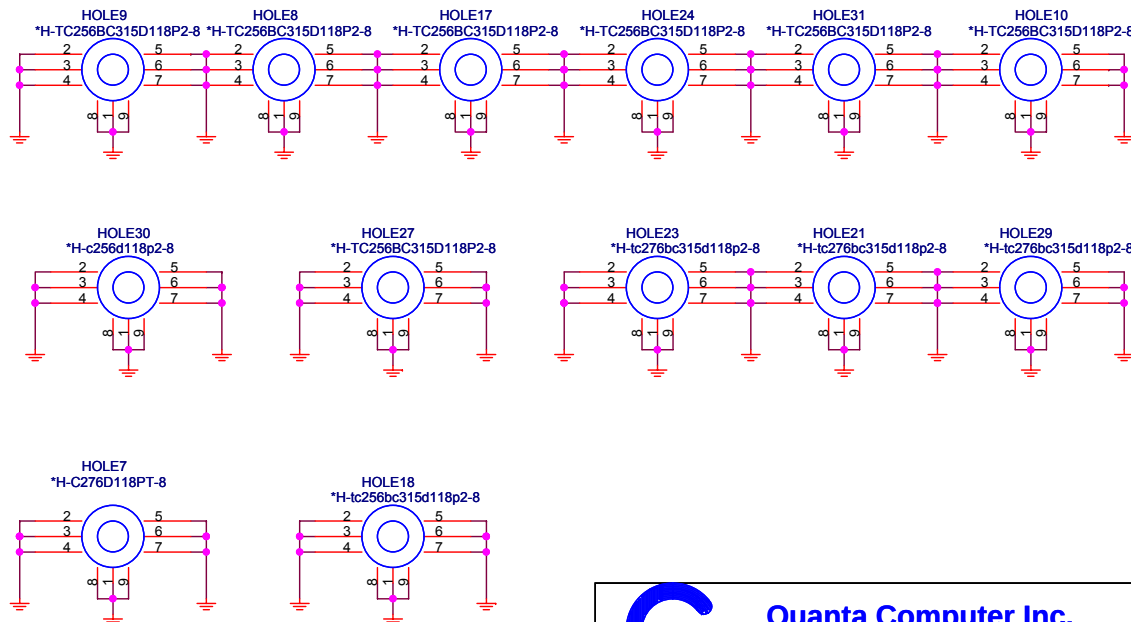


10/16: Change BOM



USBP0- R	D47	2	1	MLVG06031R
USBP0+ R	D48	2	1	MLVG06031R
USBP1- R	D49	2	1	MLVG06031R
USBP1+ R	D50	2	1	MLVG06031R

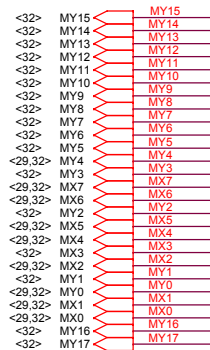
REV:C Modify



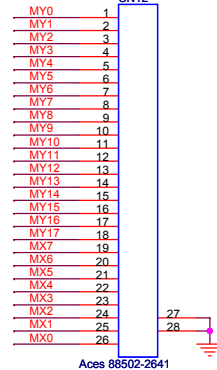
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	USB/FINGER PRINTER	1A
Date:	Wednesday, April 09, 2008	Sheet 30 of 40

INT K/B

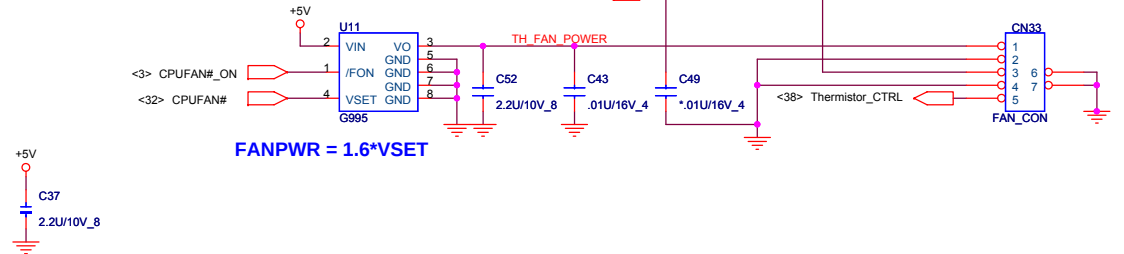


Rev:B change footprint



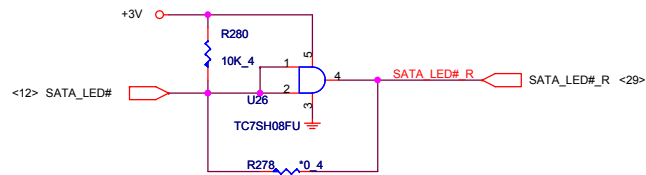
Aces 88502-2641

CPU FAN



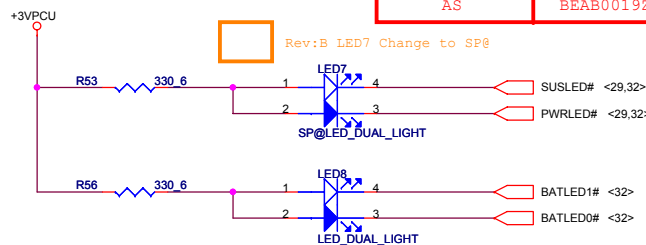
FANPWR = 1.6*VSET

LED



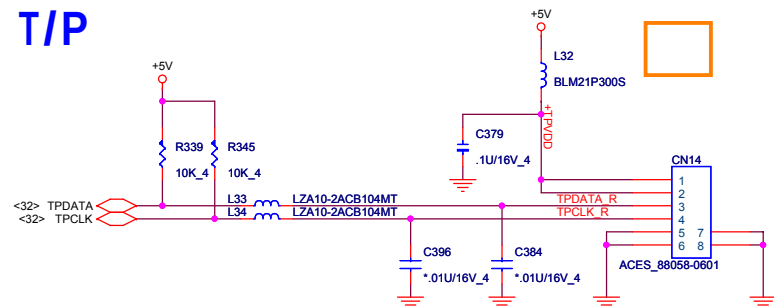
TM & LOW COST	BEGA0017ZA0
AS	BEAB0019ZA0

Rev:B LED7 Change to SP@

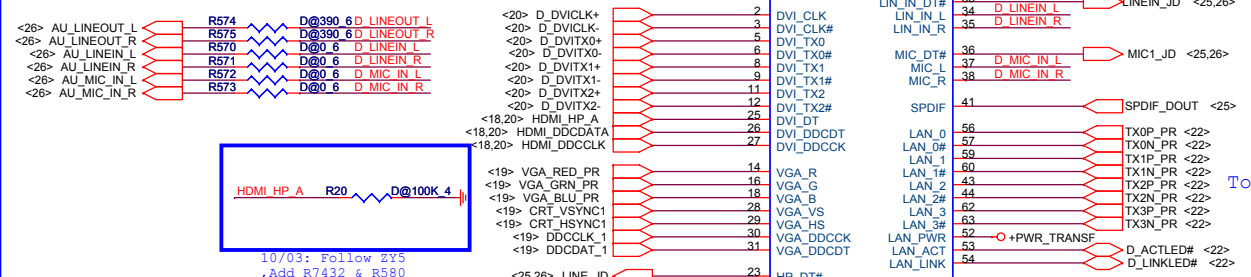


T/P

REV:B, CN14 change footprint

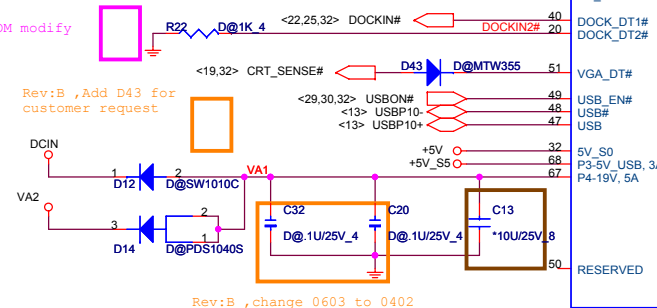


CABLE DOCK



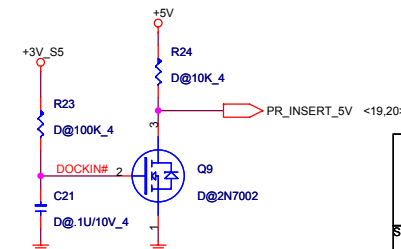
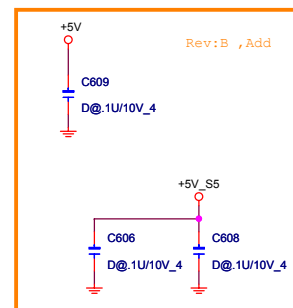
10/03: Follow ZY5, Add R7432 & R580

10/12 : BOM modify



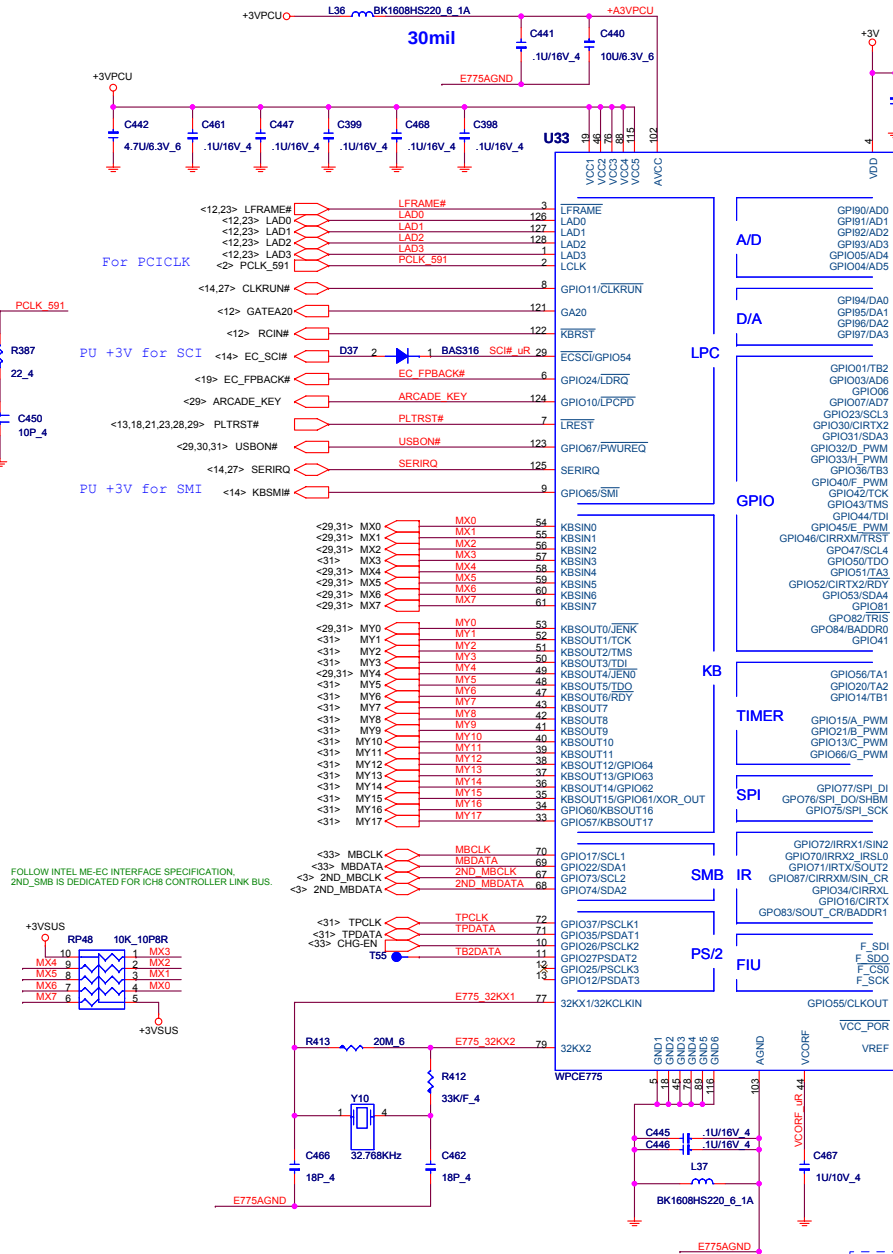
Rev:B , change 0603 to 0402

Rev:C , change 1208 to 0805

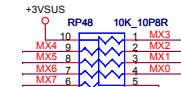


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

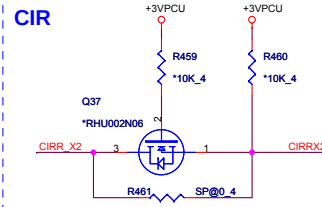
Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	1A
Date:	Wednesday, April 09, 2008	Sheet 31 of 40



FOLLOW INTEL ME-EC INTERFACE SPECIFICATION.
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.



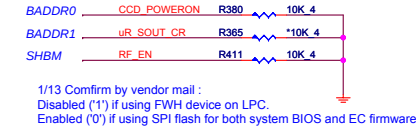
08/10 FAE:
L43 CAN CHANGE FROM BEAD TO
SHORT.
BUT, PLEASE PUT AGND & 32K CAP &
AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.



I/O ADDRESS SETTING

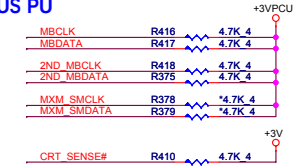
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

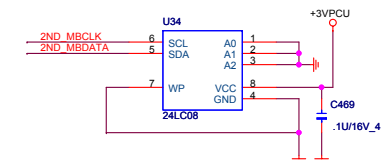


1/13 Confirm by vendor mail :
Disabled (*) if using FW device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

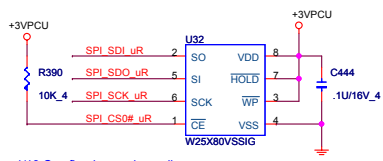
SM BUS PU



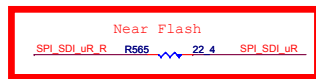
ACER ID



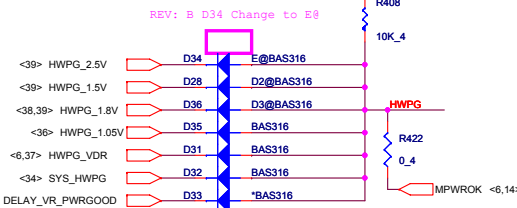
SPI FLASH



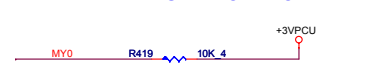
1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)

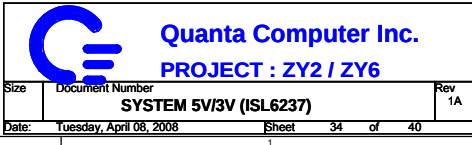


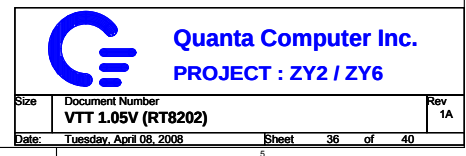
H/W POWER GOOD

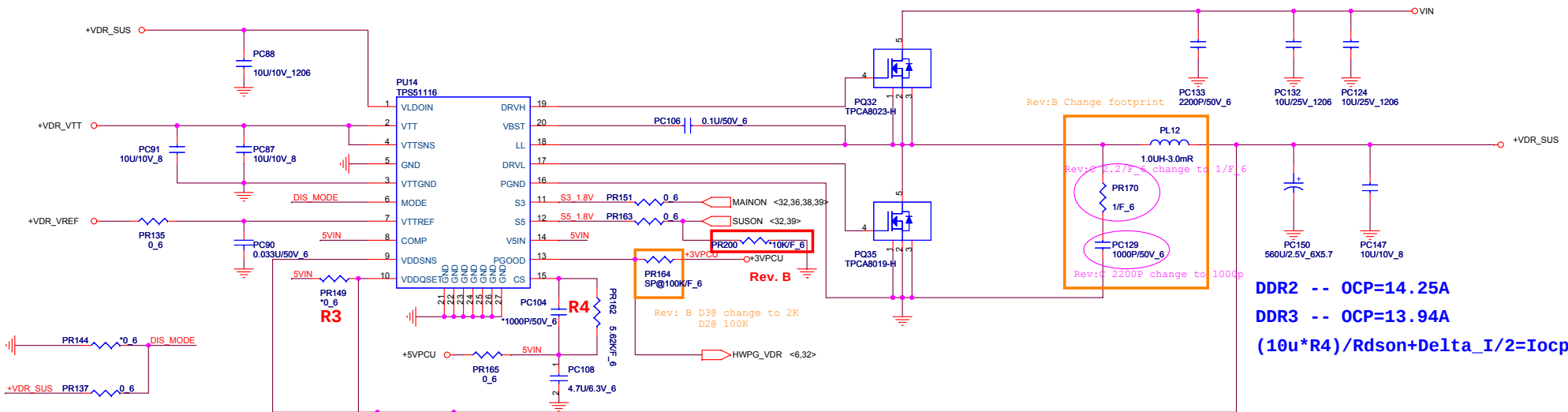


INTERNAL KEYBOARD STRIP SET







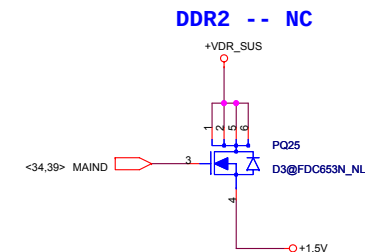
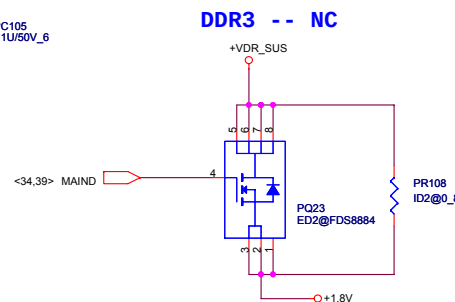


DDR2 -- OCP=14.25A
 DDR3 -- OCP=13.94A
 $(10u \cdot R4) / R_{dson} + \Delta I / 2 = I_{ocp}$

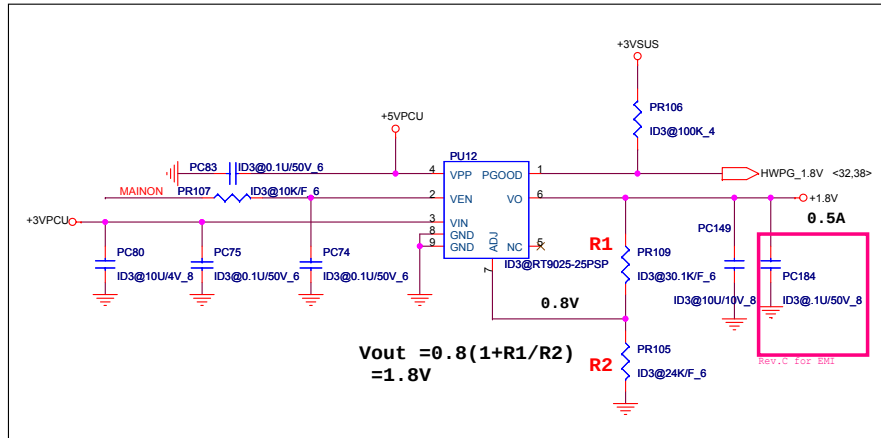
	DDR2(1.8V)	DDR3(1.5V)
R1	76.8K CS37683F927	75K CS37503F919
R2	110K CS41103F910	76.8K CS37683F927

$$R1 = (100 \cdot V_{out} - R2)K$$

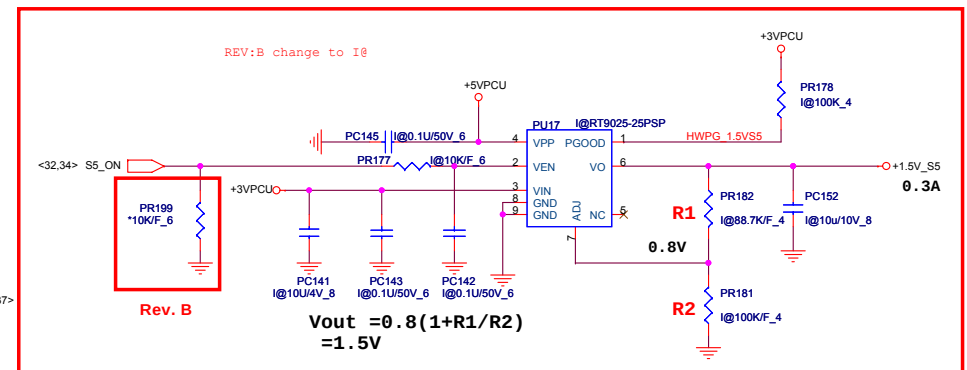
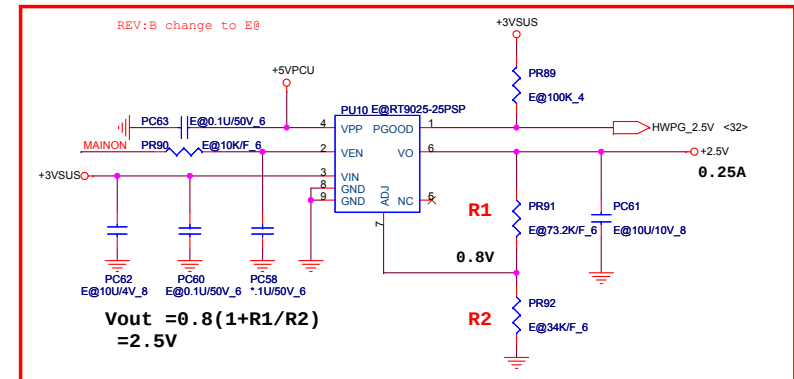
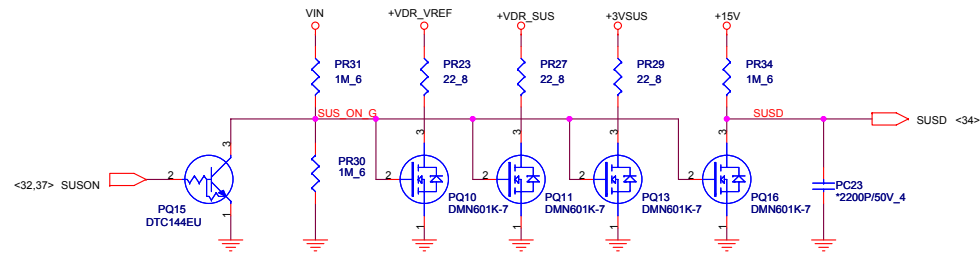
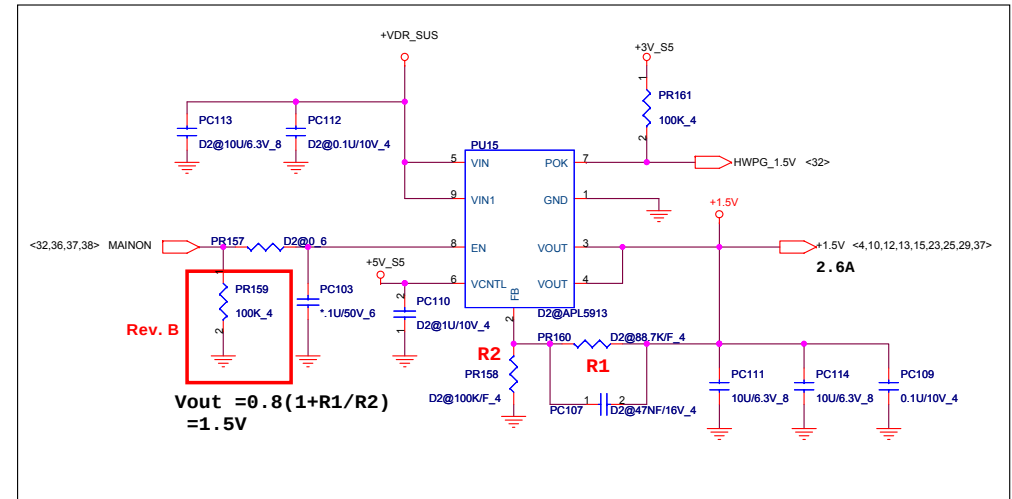
if tune Vout R3 un-mount, R1 and R2 mount



for DDR3 and UMA

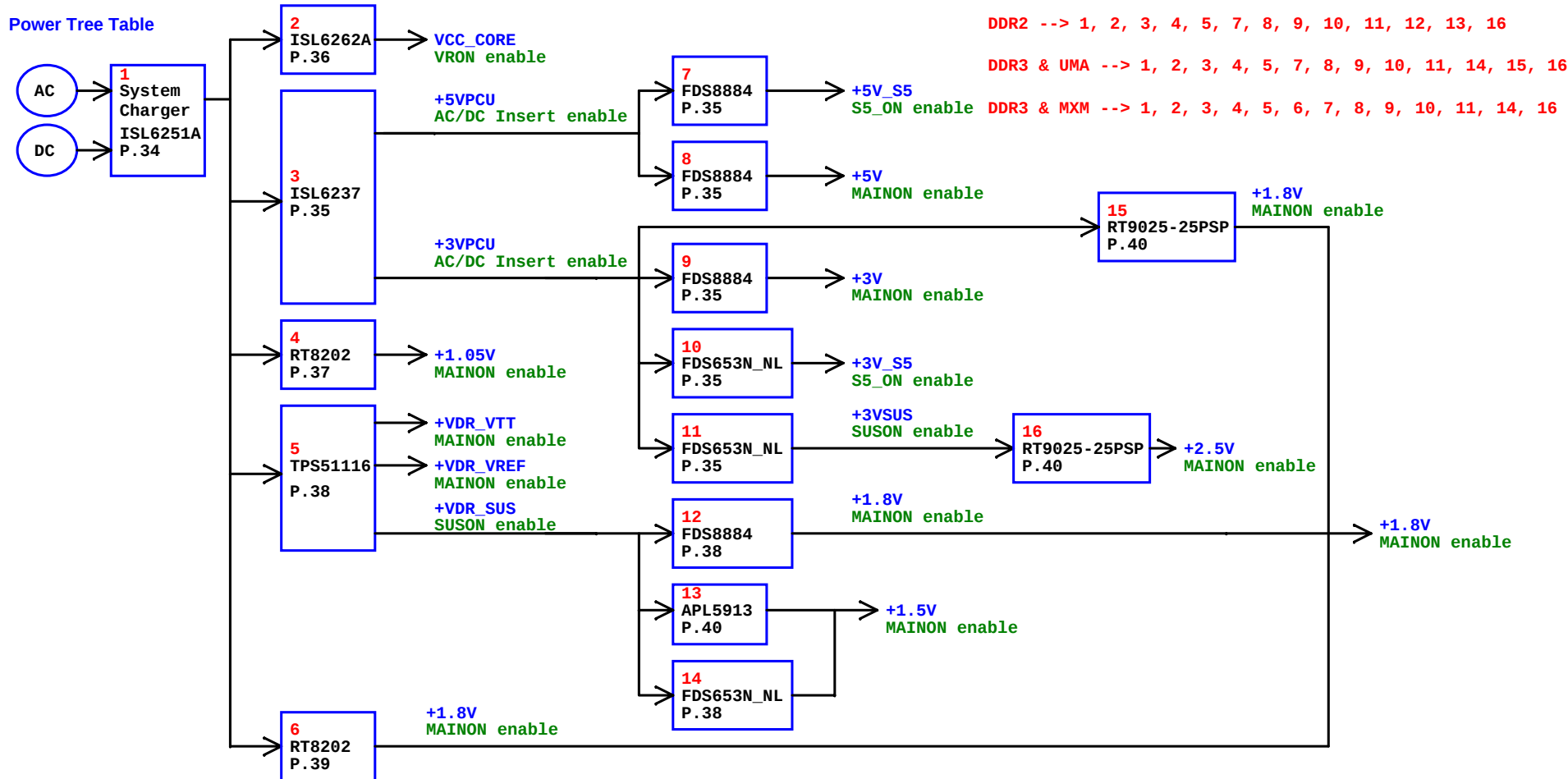


DDR3 -- NC



REV:B change to E@

Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129)
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Model	REV	CHANGE LIST	MODEL	ZY2	
				FROM	To
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)		X	1A
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)		X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
	2A	Page19 : change U22 LVDS PWR SW IC to TI for display issue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 :change U13 packing from TQFN to TDFN for vendor request		1A	2A
	2B	Page20 : Add		1A	2A
				1A	2A
				1A	2A
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2B	3A
				2B	3A
				2B	3A
				2B	3A
				2B	3A